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EE115 Analog Circuits
Non-Ideal Op Amp

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Outline

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- Non-Ideal Op Amp
  - DC Imperfections
  - Finite Open-Loop Gain and Bandwidth
  - Large-Signal Operation of Op Amps
- Reading: SEDTRA/SMITH book pages 97-116

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Review: Ideal Op-Amp

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- Infinite input impedance
  - No current goes in, **virtual open circuit**
- Zero output impedance
- Infinite open-loop gain, A
  - **Virtual short circuit** between the inverting and non-inverting input ports
- Infinite bandwidth
- Infinite common-mode rejection
  - Common mode rejection ratio (CMRR)

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Electrical Characteristics of a Real Op-Amp

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PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	V_S = 5 V		±0.3	±1.6	mV
		V_S = 5 V, T_A = –40°C to 125°C			±2	
dV_{OS}/dT	Drift	V_S = 5 V, T_A = –40°C to 125°C		±0.53		µV/°C
PSRR	Power-supply rejection ratio	V_S = 1.8 V – 5.5 V, V_{CM} = (V–)		±7	±80	µV/V
	Channel separation, DC	At DC		100		dB
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range	V_S = 1.8 V to 5.5 V	(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	V_S = 5.5 V, (V–) – 0.1 V < V_{CM} < (V+) – 1.4 V, T_A = –40°C to 125°C	80	103		dB
		V_S = 5.5 V, V_{CM} = –0.1 V to 5.6 V, T_A = –40°C to 125°C	57	87		
		V_S = 1.8 V, (V–) – 0.1 V < V_{CM} < (V+) – 1.4 V, T_A = –40°C to 125°C		88		
		V_S = 1.8 V, V_{CM} = –0.1 V to 1.9 V, T_A = –40°C to 125°C		81		
INPUT BIAS CURRENT						
I_B	Input bias current			±0.5		pA
I_{OS}	Input offset current			±0.05		pA
NOISE						
E_n	Input voltage noise (peak-to-peak)	V_S = 5 V, f = 0.1 Hz to 10 Hz		4.77		μV_{PP}
e_n	Input voltage noise density	V_S = 5 V, f = 10 kHz		10		$nV/\sqrt{Hz}$
		V_S = 5 V, f = 1 kHz		16		
i_n	Input current noise density	f = 1 kHz		23		$fA/\sqrt{Hz}$
INPUT CAPACITANCE						
C_{ID}	Differential			2		pF
C_{IC}	Common-mode			4		pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	V_S = 1.8 V, (V–) + 0.04 V < V_O < (V+) – 0.04 V, R_L = 10 kΩ		100		dB
		V_S = 5.5 V, (V–) + 0.05 V < V_O < (V+) – 0.05 V, R_L = 10 kΩ	104	130		
		V_S = 1.8 V, (V–) + 0.06 V < V_O < (V+) – 0.06 V, R_L = 2 kΩ		100		
		V_S = 5.5 V, (V–) + 0.15 V < V_O < (V+) – 0.15 V, R_L = 2 kΩ		130		

TLV9064I, 5.5-V, 10-MHz, operational amplifier

Switching Characteristics of a Real Op-Amp

FREQUENCY RESPONSE				
GBP	Gain bandwidth product	V_S = 5 V, G = +1	10	MHz
φ_m	Phase margin	V_S = 5 V, G = +1	55	°
SR	Slew rate	V_S = 5 V, G = +1	6.5	V/μs
t_S	Settling time	To 0.1%, V_S = 5 V, 2-V step , G = +1, C_L = 100 pF	0.5	μs
		To 0.01%, V_S = 5 V, 2-V step, G = +1, C_L = 100 pF	1	
t_{OR}	Overload recovery time	V_S = 5 V, V_{IN} × gain > V_S	0.2	μs
THD + N	Total harmonic distortion + noise(1)	V_S = 5.5 V, V_{CM} = 2.5 V, V_O = 1 V_{RMS}, G = +1, f = 1 kHz	0.0008%	
OUTPUT				
V_O	Voltage output swing from supply rails	V_S = 5.5 V, R_L = 10 kΩ	20	mV
		V_S = 5.5 V, R_L = 2 kΩ	60	
I_{SC}	Short-circuit current	V_S = 5 V	±50	mA
Z_O	Open-loop output impedance	V_S = 5 V, f = 10 MHz	100	Ω

Imperfections in Practical Op-Amps

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- Finite open-loop gain ($A_o < \infty$)
- Finite input resistance ($R_i < \infty$)
- Non-zero output resistance ($R_o > 0$)
- Finite bandwidth
- Offset voltage
- Input bias and offset currents

Offset Voltage

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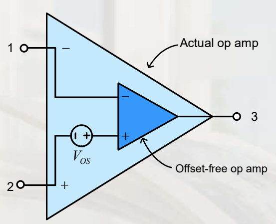

Fig. Circuit model for an op amp with input offset voltage V_{OS}.

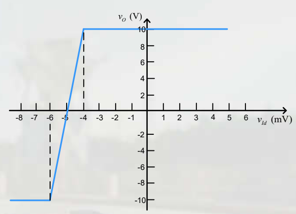

Fig. Transfer characteristic of an op amp with V_{OS} = 5 mV and output saturation levels ±10 V.

Causes: mismatches in the input differential stage

Trimming of Offset Voltage

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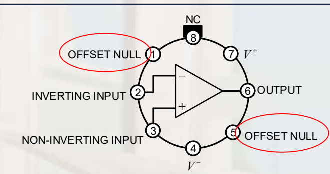


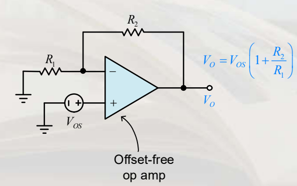


Fig. Evaluating the output dc offset voltage due to V_{OS} in a closed-loop amplifier.

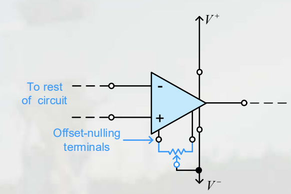
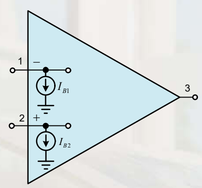


Fig. output dc offset voltage of an op amp can be trimmed to zero by connecting a potentiometer to the two offset-nulling terminals.

Input Bias Currents and Offset Currents*



- **Input bias current:**

$$I_B = (I_{B1} + I_{B2})/2$$

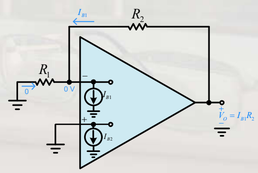
- **Input offset current**

$$I_{OS} = |I_{B1} - I_{B2}|$$

- Typical CMOS Op amps:
  - I_B < 1 pA
  - I_{OS} < 0.1 pA

How to measure I_B?

$$V_O = I_{B1}R_2 \cong I_B R_2$$



Reducing the Effect of Input Bias Currents *

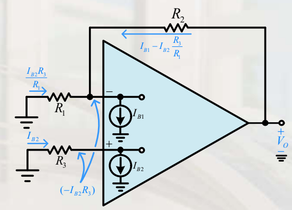


Fig. Reducing the effect of the input bias currents by introducing a resistor R_3.

Introduce R_3 in series with the non-inverting input

$$V_o = -I_{B2}R_3 + R_2(I_{B1} - I_{B2}R_3/R_1) *$$

If $I_{B1} = I_{B2} = I_B$,

$$V_o = I_B[R_2 - R_3(1 + R_2/R_1)]$$

Reduce V_o to 0 by designing R_3

$$R_3 = \frac{R_2}{1 + R_2/R_1} = \frac{R_1R_2}{R_1 + R_2}$$

Insert into *,

$$V_o = I_{OS}R_2$$

Frequency Response of Open-Loop Op Amp

- **Single pole response** with a dominant pole at ω_b

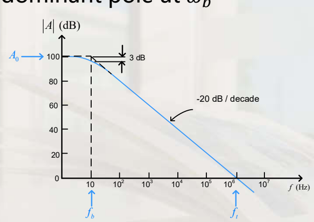


Fig. Open-loop gain of a typical general-purpose, internally compensated op amp.

- Open-loop transfer function

$$A(j\omega) = \frac{A_o}{1 + j\omega/\omega_b}$$

- At higher frequency

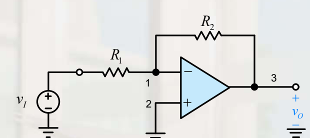
$$A(j\omega) \cong \frac{A_o\omega_b}{j\omega}$$

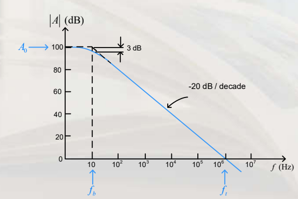
$$|A(j\omega)| = \frac{A_o\omega_b}{\omega}$$

- Unity-gain bandwidth

$$\omega_t = A_o\omega_b$$

Frequency Response of Closed-Loop Op Amp (Inverting Amplifier Example)





- Close-loop transfer function:

$$\frac{V_o}{V_i} = \frac{-R_2/R_1}{1 + (1 + R_2/R_1)/A}$$

- Include the bandwidth-limited A:

$$A(s) = \frac{A_o}{1 + s/(\omega_t/A_o)} = \frac{A_o}{1 + A_o s/\omega_t}$$

$$\frac{V_o(s)}{V_i(s)} = \frac{-R_2/R_1}{1 + \frac{1}{A_o}(1 + R_2/R_1) + \frac{s}{\omega_t/(1 + R_2/R_1)}}$$

- If: $A_o \gg 1 + R_2/R_1$,

$$\frac{V_o(s)}{V_i(s)} \cong \frac{-R_2/R_1}{1 + \frac{s}{\omega_t/(1 + R_2/R_1)}}$$

- Close-loop corner frequency:

$$\omega_{3dB} = \frac{\omega_t}{1 + R_2/R_1}$$

- **GBW** unchanged

Frequency Response of Closed-Loop (Noninverting Amplifier Example)

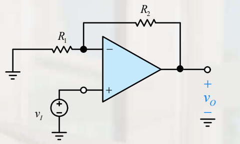
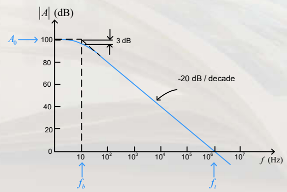


Figure 2.12 The noninverting configuration.



- Close-loop transfer function:

$$\frac{V_o}{V_i} = \frac{1+R_2/R_1}{1+(1+R_2/R_1)/A}$$

- Include the bandwidth-limited A:

$$A(s) = \frac{A_o}{1+s/(\omega_t/A_o)}$$

$$\frac{V_o(s)}{V_i(s)} \cong \frac{1+R_2/R_1}{1+\frac{s}{\omega_t/(1+R_2/R_1)}}$$

- Close-loop corner frequency:

$$\omega_{3dB} = \frac{\omega_t}{1+R_2/R_1}$$

- **GBW** unchanged

Output Saturation

- The output voltage swing is limited by
  - 1. **Saturation voltage** (usually 1~2V lower than power supply voltage)
  - 2. **Maximum output current** (in case of small load resistance)
- Output waveform appears to be "clipped" when either condition happens

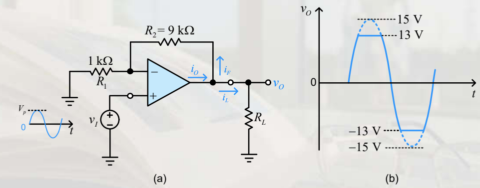


Fig. (a) A noninverting amplifier with a nominal gain of 10 V/V designed using an op amp that saturates at ±13-V output voltage and has ±20-mA output current limits. **(b)** When the input sine wave has a peak of 1.5 V, the output is clipped off at ±13 V.

Slew Rate

- Amplifier output is limited by "**slew rate**": maximum rate of change possible at output

$$SR = \left.\frac{dv_o}{dt}\right|_{max}$$

- SR is specified in datasheet in V/μs.
- Note: SR limit is different from bandwidth limit:
  - Limited **bandwidth** is a **linear** phenomenon, it does not result in changing the shape of an input sinusoid
  - **SR** limitation can cause **nonlinear** distortion to input sinusoidal signal.

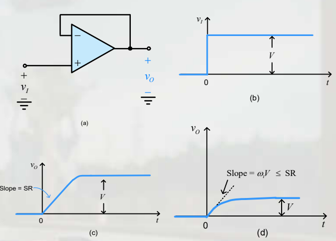
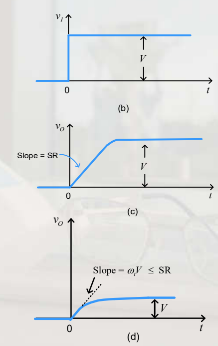


Fig. (a) Unity-gain follower. **(b)** Input step waveform. **(c)** Linearly rising output waveform obtained when the amplifier is slew-rate limited. **(d)** Exponentially rising output waveform obtained when V is sufficiently small so that the initial slope ($\omega_t V$) is smaller than or equal to SR.

Comparison of Slew Rate and Bandwidth Limits

- For a **step response,** both SR and bandwidth limits cause the output to rise with a finite slope, but there is an important difference:
- Slew rate limited output:
  - Slope = SR at all times
- Bandwidth limited output:
  - $Slope = \omega_t V exp(-\omega_t t) < SR$
- (V: steady state output voltage)



- Transfer function:

$$\frac{V_o(s)}{V_i(s)} = \frac{1}{1+\frac{s}{\omega_t}}$$

- Time domain:

$$v_o(t) = V(1-e^{-\omega_t t})$$

Full-Power Bandwidth

- For sinusoidal input to unity-gain follower:

$$v_I = V_i \sin \omega t$$

- Rate of change:

$$\frac{dv_I}{dt} = V_i \omega \cos \omega t \le SR$$

- **Full-power bandwidth**:
  The frequency at which SR-limited distortion starts to occur for an output sinusoid with maximum rated output voltage, V_{omax},

$$\omega_M V_{omax} = SR$$

$$f_M = \frac{SR}{2\pi V_{omax}}$$

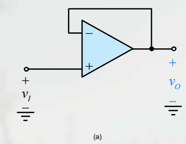


Fig. (a) Unity-gain follower.

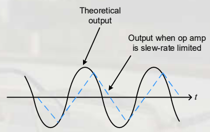


Fig. Effect of slew-rate limiting on output sinusoidal waveforms.

Summary

- Open loop gain
- Input impedance
- Output impedance
- Input offset & Bias
- CMRR
- Saturation
- Unity-gain bandwidth
- Slew rate
- Full-power bandwidth