EE115A Analog Circuits

Homework 4

Due date: 11/4/2025

Note:

- Please provide enough calculation process to get full marks.
- Please submit your homework to Gradescope (code **J62G3D**) in PDF version.
- It's highly recommended to write every exercise on a single sheet of page.
- Late submissions will have points deducted according to the penalty policy.
- Please use English only to complete the assignment, solutions in Chinese are not allowed.
- Plagiarizer will get zero points.
- The full score of this assignment is 100 points.

Exercise 1. (20pt)

Consider the MOSFET amplifier of **Fig.P1** for the case V_t = 0.4 V, kn = 10 mA/V^2, V_{GS} = 0.6 V, V_{DD} = 1.8 V, and R_D = 6.8 kΩ.

(a) Find the dc quantities I_D and V_{DS}
(b) Calculate the value of g_m at the bias point.
(c) Calculate the value of the voltage gain.

(d) If the MOSFET has $\lambda = 0.2\ V^{-1}$, find r_o, at the bias point

and calculate the voltage gain.

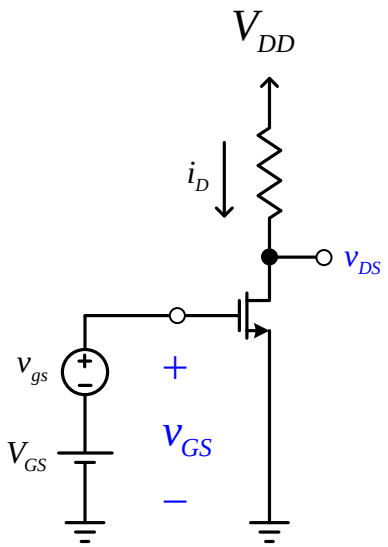

Fig.P1

Exercise 2. (20pt)

In the circuit of **Fig.P2**, the NMOS transistor has $|Vt|$ = 0.8 V and V_A = 20 V and operates with VD = 1V. What is the voltage gain vo/vi? What do V_D and the gain become for I increased to 1 mA?

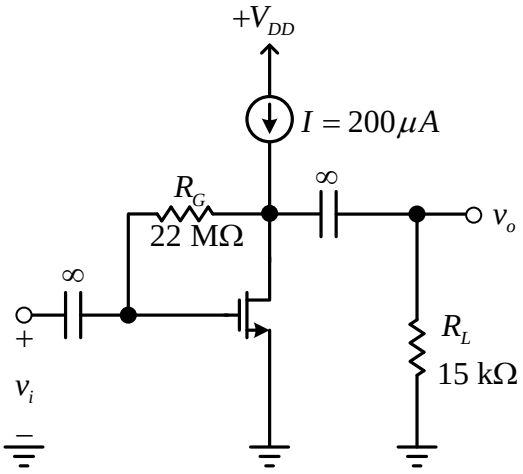

Fig.P2

Exercise 3. (20pt)

A CS amplifier utilizes a MOSFET with $\mu_n C_{ox}$ = 400μA/V^2 and WL = 10. It is biased at I_D = 0.5 mA and uses R_D = 10kΩ. Find R_{in}, A_{vo}, and R_o. Also, if a load resistance of 10 kΩ is connected to the output, what overall voltage gain G_V is realized? Now, if a 0.5-V peak sine-wave signal is required at the output, what must the peak amplitude of v_{sig} be?

Exercise 4. (20pt)

Design the circuit of **Fig.P4** for a MOSFET having $Vt = 0.6$ V and $kn = 5$ mA/V^2. Let $V_{DD} = V_{SS} = 3$ V. Design for a dc bias current of 0.4 mA and for the largest possible voltage gain (and thus the largest possible R_D) consistent with allowing a 1.2-V peak-to-peak voltage swing at the drain. Assume that the signal voltage on the source terminal of the FET is zero.

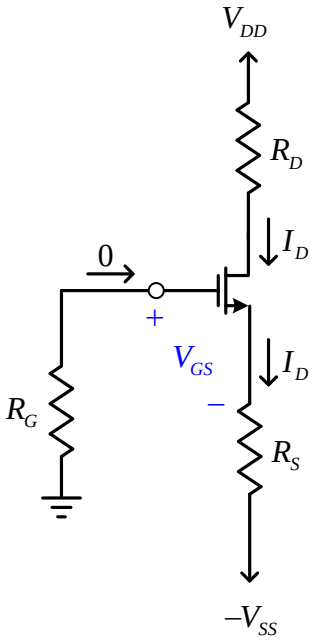

Fig.P4

Exercise 5. (20pt)

Note: This question requires simulation. Please note that you need to use Multisim for simulation and provide the simulation circuit and simulation results in your answer.

Ensure that you provide both theoretical calculation results and simulation results.

The PMOS transistor in the CS amplifier of **Fig.P6** has *Vtp* = —0.75 V and a very large | *VA* |.

(a) Select a value for *Rs*. to bias the transistor at I_D = 0.5 mA and |Vov| = 0.25 V. Assume v_{sig} to have a zero dc component.
(b) Select a value for R_D that results in *Gv* = —12 V/V.

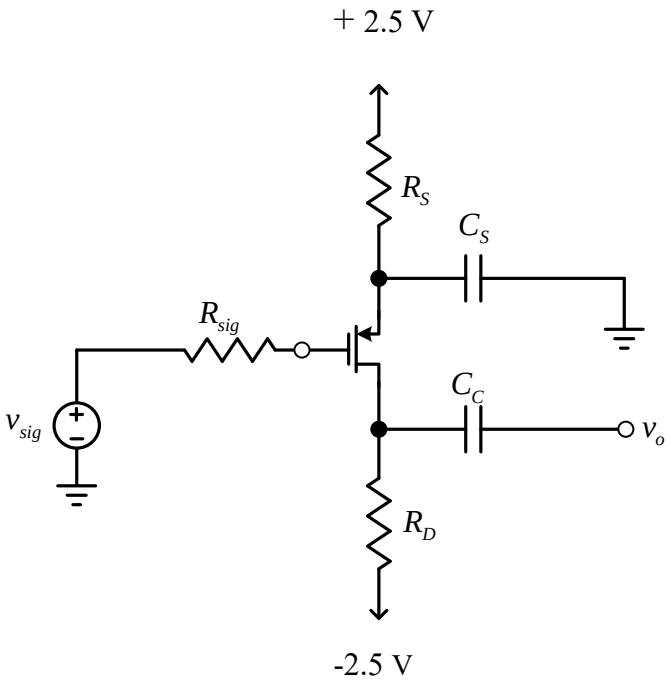

Fig.P5