

# EE115A Analog Circuits

## Homework 5

Due date: **25/11/2025**

**Note:**

- Please provide enough calculation process to get full marks.
- Please submit your homework to Gradescope (code **J62G3D**) in PDF version.
- It's highly recommended to write every exercise on a single sheet of page.
- Late submissions will have points deducted according to the penalty policy.
- Please use English only to complete the assignment, solutions in Chinese are not allowed.
- Plagiarizer will get zero points.
- The full score of this assignment is 100 points.

### Exercise 1. (15pt)

The current-steering circuit of Fig. P1 is fabricated in a CMOS technology for which  $\mu_n C_{ox} = 400 \mu\text{A}/\text{V}^2$ ,  $\mu_p C_{ox} = 100 \mu\text{A}/\text{V}^2$ ,  $V_{tn} = 0.5 \text{ V}$ ,  $V_{tp} = -0.5 \text{ V}$ ,  $V'_{A_n} = 6 \text{ V}/\mu\text{m}$ , and  $|V'_{A_p}| = 6 \text{ V}/\mu\text{m}$ . If all devices have  $L = 0.5 \mu\text{m}$ , design the circuit so that  $I_{REF} = 20 \mu\text{A}$ ,  $I_2 = 80 \mu\text{A}$ ,  $I_3 = I_4 = 50 \mu\text{A}$ , and  $I_5 = 100 \mu\text{A}$ . Use the minimum possible device widths needed to operate the current source  $Q_2$  with voltages at its drain as high as  $+0.8 \text{ V}$  and to operate the current sink  $Q_5$  with voltages at its drain as low as  $-0.8 \text{ V}$ . Specify the widths of all devices and the value of  $R$ . Find the output resistance of the current source  $Q_2$  and the output resistance of the current sink  $Q_5$ .

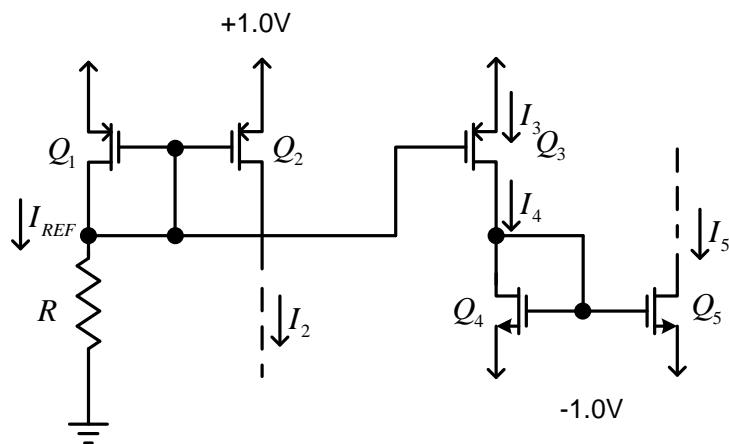


Fig. P1

## Exercise 2. (15pt)

Consider an NMOS transistor fabricated in a  $0.18\text{-}\mu\text{m}$  technology for which  $k_n' = 400 \mu\text{A/V}^2$  and  $V_A' = 5 \text{ V}/\mu\text{m}$ . It is required to obtain an intrinsic gain of  $25 \text{ V/V}$  and a  $g_m$  of  $1 \text{ mA/V}$ . Using  $V_{ov} = 0.2 \text{ V}$ , find the required values of  $L$ ,  $W/L$ , and the bias current  $I$ .

### Exercise 3. (20pt)

The purpose of this problem is to investigate the signal currents and voltages at various points throughout a cascode amplifier circuit. Knowledge of this signal distribution is very useful in designing the circuit so as to allow for the required signal swings. Figure P3 shows a CMOS cascode amplifier with all dc voltages replaced with signal grounds. As well, we have explicitly shown the resistance  $r_o$  of each of the four transistors. For simplicity, we are assuming that the four transistors have the same  $g_m$  and  $r_o$ . The amplifier is fed with a signal  $v_i$ .

- Determine  $R_1$ ,  $R_2$ , and  $R_3$ . Assume  $g_m r_o \gg 1$ .
- Determine  $i_1$ ,  $i_2$ ,  $i_3$ ,  $i_4$ ,  $i_5$ ,  $i_6$ , and  $i_7$ , all in terms of  $v_i$ . (Hint: Use the current-divider rule at the drain of  $Q_1$ .)
- Determine  $v_1$ ,  $v_2$ , and  $v_3$ , all in terms of  $v_i$ .
- If  $v_i$  is a 5-mV peak sine wave and  $g_m r_o = 20$ , sketch and clearly label the waveforms of  $v_1$ ,  $v_2$ , and  $v_3$ .

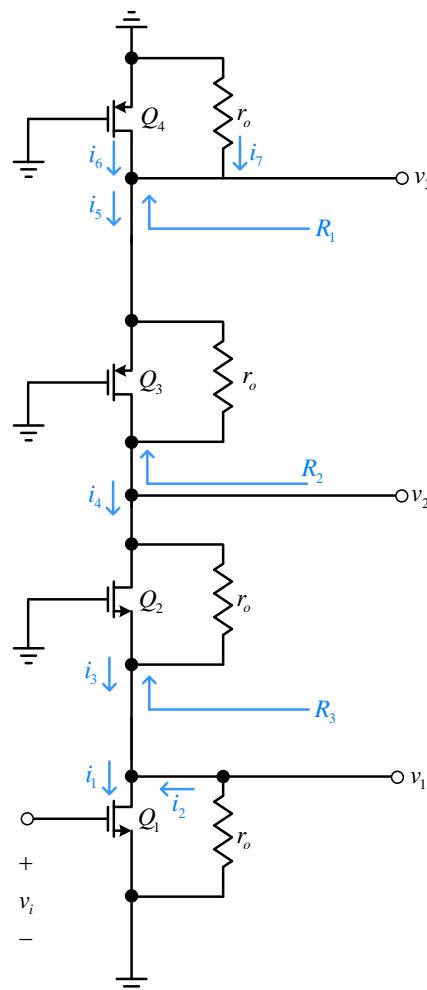


Figure P3

### Exercise 4. (15pt)

A source follower for which  $k_n' = 400 \mu\text{A}/\text{V}^2$ ,  $V_A' = 9 \text{ V}/\mu\text{m}$ ,  $\chi = 0.2$ ,  $L = 0.6 \mu\text{m}$ ,  $W = 12 \mu\text{m}$ , and  $V_t = 0.5 \text{ V}$  is required to provide a dc level shift (between input and output) of 0.8 V.

(a) What must the bias current be?

(b) Find  $g_m$ ,  $g_{mb}$ ,  $r_o$ ,  $A_{vo}$ , and  $R_o$ . Assume that the bias current source has an output resistance equal to  $r_o$ . Also find the voltage gain when a load resistance of  $3 \text{ k}\Omega$  is connected to the output.

## Exercise 5. (35pt)

Note: This question requires simulation. Please note that you need to use [Multisim](#) for simulation and provide the simulation circuit and simulation results in your answer.

Ensure that you provide both [theoretical calculation](#) results and [simulation](#) results.

A particular cascoded NMOS current mirror, such as that shown in Fig. P5, is fabricated in the  $0.18\text{-}\mu\text{m}$  CMOS process specified in Table 1. All transistors have equal channel lengths  $L = 0.54\text{ }\mu\text{m}$ . Width  $W_1 = W_4 = 2.7\text{ }\mu\text{m}$ , and  $W_2 = W_3 = 27\text{ }\mu\text{m}$ . The reference current  $I_{REF}$  is  $20\text{ }\mu\text{A}$ .

- (a) What output current results?
- (b) What are the voltages at the gates of  $Q_2$  and  $Q_3$ ?
- (c) What is the lowest voltage at the output for which proper current-source operation is possible?
- (d) What are the values of  $g_m$  and  $r_o$  of  $Q_2$  and  $Q_3$ ?
- (e) What is the output resistance of the mirror?

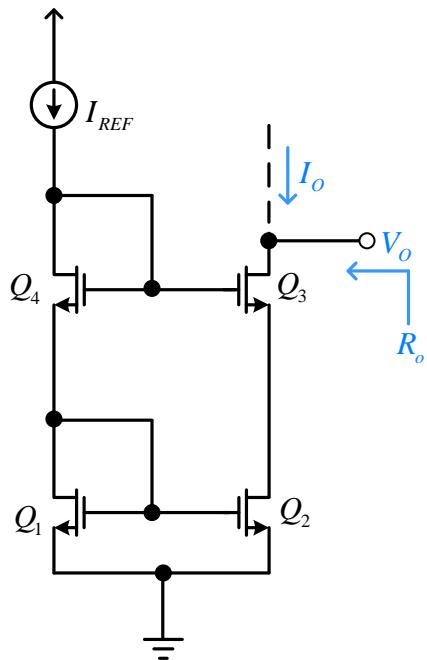


Fig. P5

Table 1:

Parameter (0.18 $\mu$ m)	NMOS	PMOS
$t_{ox}$ (nm)	4	4
$c_{ox}$ (fF/ $\mu$ m $^2$ )	8.6	8.6
$\mu$ (cm $^2$ /V $\cdot$ s)	450	100
$\mu c_{ox}$ ( $\mu$ A/V $^2$ )	387	86
$V_{t0}$ (V)	0.5	-0.5
$V_{DD}$ (V)	1.8	1.8
$ V_{A'} $ (V/ $\mu$ m)	5	6
$C_{ov}$ (fF/ $\mu$ m)	0.37	0.33