EE115A Analog Circuits

Homework 7

Due date: 12/11/2025

Note:

- Please provide enough calculation process to get full marks.
- Please submit your homework to Gradescope (code **J62G3D**) in PDF version.
- It's highly recommended to write every exercise on a single sheet of page.
- Late submissions will have points deducted according to the penalty policy.
- Please use English only to complete the assignment, solutions in Chinese are not allowed.
- Plagiarizer will get zero points.
- The full score of this assignment is 100 points.

Exercise 1. (20pt)

The two-stage CMOS op amp in Fig. P1 is fabricated in a 0.18-μm technology having $k'_n = 4k'_p = 400\mu\text{A/V}^2$, $V_{tn} = -V_{tp} = 0.4\text{V}$.

(a) With A and B grounded, perform a dc design that will result in each of Q_1, Q_2, Q_3, and Q_4 conducting a drain current of 100 μA and each of Q_6 and Q_7 a current of 200 μA. Design so that all transistors operate at 0.2-V overdrive voltages. Specify the W/L ratio required for each MOSFET. Present your results in tabular form. What is the dc voltage at the output (ideally)?

(b) Find the input common-mode range.

(c) Find the allowable range of the output voltage.

(d) With $v_A = v_{id}/2$ and $v_B = -v_{id}/2$, find the voltage gain v_o/v_{id}. Assume an Early voltage of 6 V.

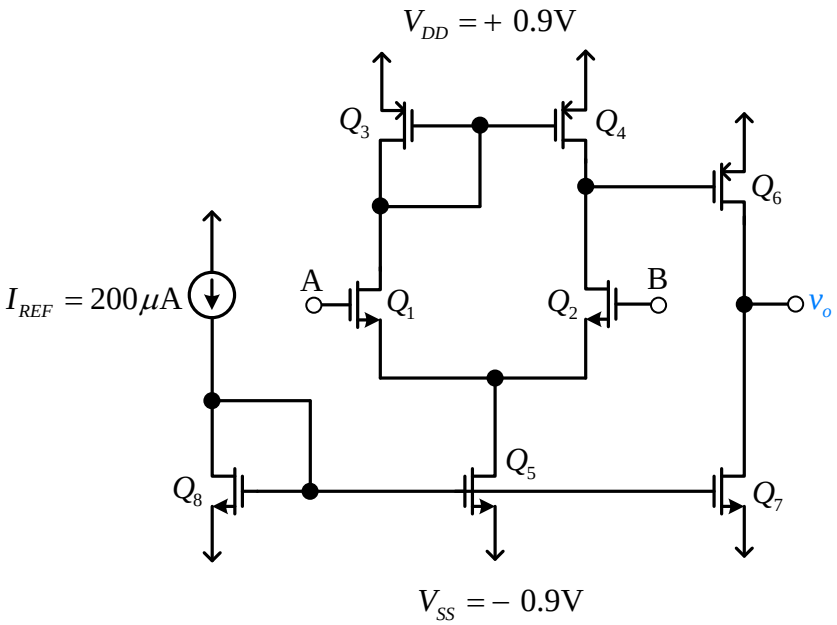


Fig. P1

Exercise 2. (20pt)

The two-stage op amp in **Figure P1(show in Exercise 1)** is fabricated in a 65-nm technology having $k'_n = 5.4 \times k'_p = 540\ \mu\text{A/V}^2$ and $V_{tn} = -V_{tp} = 0.35\ \text{V}$. The amplifier is operated with $V_{DD} = +1.2\ \text{V}$ and $V_{SS} = 0\ \text{V}$.

(a) Perform a dc design that will cause each of Q_1, Q_2, Q_3, and Q_4 to conduct a drain current of $200\ \mu\text{A}$ and each of Q_6 and Q_7 to conduct a current of $400\ \mu\text{A}$. Design so that all transistors operate at 0.15-V overdrive voltages. Specify the W/L ratio required for each MOSFET. Present all results in a table.

(b) Find the input common-mode range.

(c) Find the allowable range of the output voltage.

(d) With $v_A = v_{id}/2$ and $v_B = -v_{id}/2$, find the voltage gain v_o/v_{id}. Assume an Early voltage of $2.4\ \text{V}$.

Exercise 3. (20pt)

Find the intrinsic gain A_0 and the unity-gain frequency f_T of an n-channel transistor fabricated in a 0.13-μm CMOS process for which $L_{ov} = 0.1L$, $\mu_n = 400\,\text{cm}^2/\text{V}\cdot\text{s}$, and $V'_A = 5\,\text{V}/\mu\text{m}$. The device is operated at

$$V_{ov} = 0.2\,\text{V}.$$

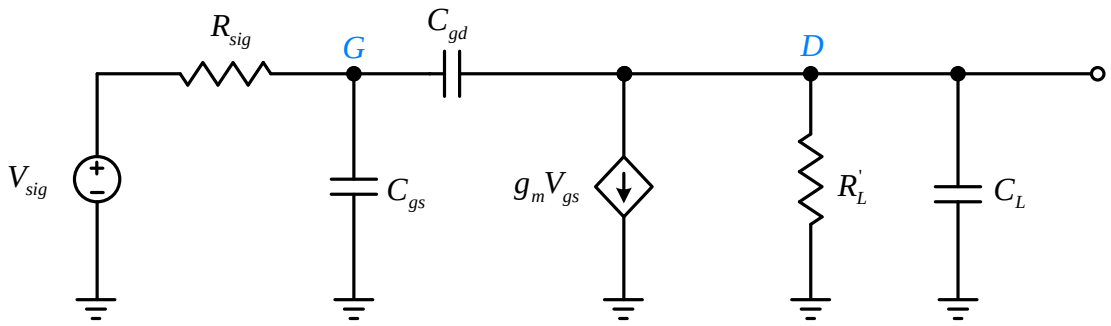
Find A_0 and f_T for devices with $L = L_{min}$, $2L_{min}$, $3L_{min}$, $4L_{min}$, and $5L_{min}$. Present your results in a table. (Hint: For f_T, use the approximate expression

$$f_T \simeq \frac{3\mu_n V_{ov}}{4\pi L^2}.)$$

Exercise 4. (20pt)

For a CS amplifier with $g_m = 5\,\text{mA/V}$, $C_{gs} = 5\,\text{pF}$, $C_{gd} = 1\,\text{pF}$, $C_L = 5\,\text{pF}$, $R_{sig} = 10\,\text{k}\Omega$, and $R_L^{'} = 10\,\text{k}\Omega$, find τ_H and f_H. What is the percentage of τ_H that is caused by the interaction of R_{sig} with the input capacitance? To what value must R_{sig} be lowered in order to double f_H?

Hint: High-frequency equivalent circuit for the CS amplifier.



Exercise 5. (20pt)

Note：This question requires simulation. Please note that you need to use Multisim for simulation and provide the simulation circuit and simulation results in your answer.

Ensure that you provide both theoretical calculation results and simulation results.

(a) Consider a CS amplifier having $C_{gd} = 0.3\,\text{pF}$, $R_{sig} = R_L = 20\,\text{k}\Omega$, $g_m = 4\,\text{mA/V}$, $C_{gs} = 2\,\text{pF}$, C_L (including C_{db}) $= 1\,\text{pF}$, $C_{db} = 0.2\,\text{pF}$, and $r_o = 20\,\text{k}\Omega$. Find the low-frequency gain A_M, and estimate f_H using open-circuit time constants. Hence determine the gain-bandwidth product.

(b) If a CG stage utilizing an identical MOSFET is cascaded with the CS transistor in (a) to create a cascode amplifier, determine the new values of A_M, f_H, and gain-bandwidth product. Assume R_L remains unchanged.

Hint: The common-gate amplifier with the transistor internal capacitances