上海科技大学
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EE115 Analog Circuits
Bias & Discrete Amp

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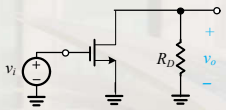
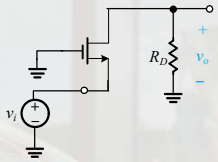
Outline

- Transistor Amplifier 3
  - Biasing
  - Discrete-Circuit Amplifiers
- Reading: SEDTRA/SMITH book pages 448-473

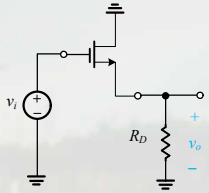
Review: Basic Single-Transistor Amp. Config.



(a) Common source (CS)



(b) Common Gate (CG)



(c) Common Drain (CD) or Source Follower

Purposes of Bias Circuit

- Provide a **stable** bias drain current
- Bias **insensitive** to variations in
  - Transistor parameters (V_t, k for MOS)
  - Temperature and other environmental changes
- Keep MOSFET in **flat part** of the I-V curves **(Saturation region)** for desired output swing

Review: I-V Curves of NMOS

$$i_D = k_n' \frac{W}{L}\left(V_{OV} v_{DS} - \frac{1}{2} v_{DS}^2\right)$$

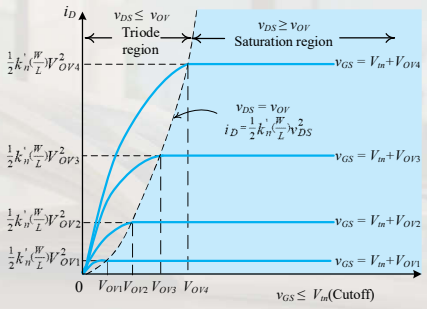
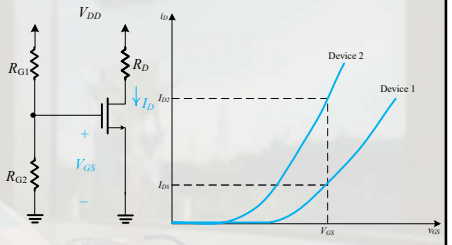


Fig. i_D - v_{DS} characteristic for an enhancement-type NMOS transistor.

$$i_D = \frac{1}{2} k_n' \frac{W}{L} V_{OV}^2$$

Example of Non-Ideal Bias

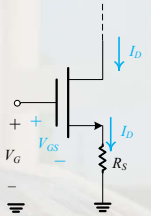
- Fixed v_{GS} from voltage divider
- Large variation in i_D due to **device** variations
- Large **temperature** dependence
  - μ_n and V_t are temperature sensitive

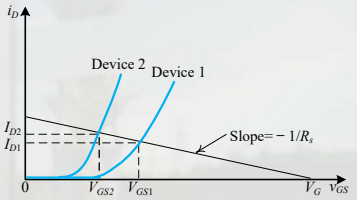


$$i_D = \frac{1}{2} \mu_n C_{OX} \frac{W}{L} (v_{GS} - V_t)^2$$

Adding Source Resistance R_S

$$V_G = V_{GS} + R_S I_D$$

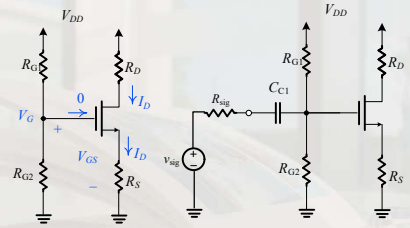




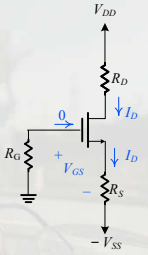
- R_S provides a **negative feedback**
  - If $I_D \uparrow$, $V_{GS} \downarrow \rightarrow I_D \downarrow$
  - If $I_D \downarrow$, $V_{GS} \uparrow \rightarrow I_D \uparrow$
- **Stabilize I_D** w.r.t. device and temperature variations

Practical Implementations

Single Power Supply



Dual Power Supply

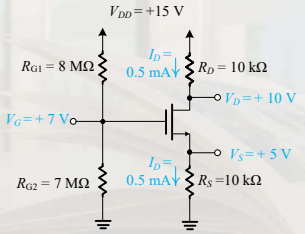


How to select R_d?

Rule of thumb: R_D, V_{D9}, and R_S each has $1/3\,V_{DD}$ voltage drop

Bias Example

Given: I_D=0.5 mA; V_t = 1V, k_n = 1 mA/V², λ = 0. V_{DD} = 15V.
Calculate change in I_D when the MOSFET is replaced with another one with identical k_n but V_t = 1.5V



Solution:

Rule of thumb: R_D, V_{DS} and R_S each has $1/3\,V_{DD}$ voltage drop

$$R_D = \frac{V_{DD} - V_D}{I_D} = \frac{15 - 10}{0.5} = 10\ \text{k}\Omega$$

$$R_S = \frac{V_S}{R_S} = \frac{5}{0.5} = 10\ \text{k}\Omega$$

$$I_D = \frac{1}{2} k'_n (W/L) V_{OV}^2$$

$$0.5 = \frac{1}{2} \times 1 \times V_{OV}^2$$

$$V_{GS} = V_t + V_{OV} = 1 + 1 = 2\ \text{V}$$

$$V_G = V_S + V_{GS} = 5 + 2 = 7\ \text{V}$$

Replace

$$I_D = \frac{1}{2} \times 1 \times (V_{GS} - 1.5)^2$$

$$V_G = V_{GS} + I_D R_S$$

$$7 = V_{GS} + 10 I_D$$

$$I_D = 0.455\ \text{mA}$$

$$\Delta I_D = 0.455 - 0.5 = -0.045\ \text{mA}$$

Bias with large drain-to-gate R_G

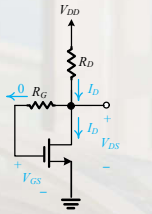


Fig. Biasing the MOSFET using a large drain-to-gate feedback resistance, R_G.

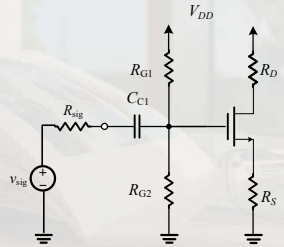
$$V_{GS} = V_{DS} = V_{DD} - R_D I_D$$

$$V_{DD} = V_{GS} + R_D I_D$$

- R_D provides a negative feedback
  - $I_D \uparrow$, $V_{GS} \downarrow \rightarrow I_D \downarrow$
  - $I_D \downarrow$, $V_{GS} \uparrow \rightarrow I_D \uparrow$
- **Stabilize I_D** w.r.t. device and temperature variations

Coupling. Cap to Separate AC Signal from DC Bias

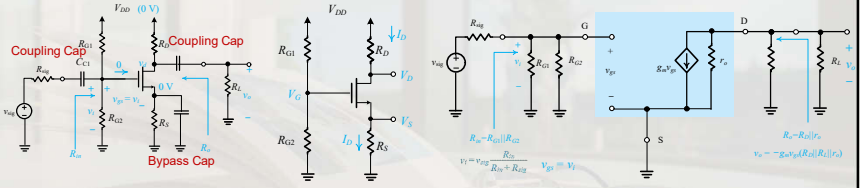
- Coupling capacitor is **DC-open** and **AC-short**
- **Prevent** signal source to **change** bias condition
- Coupling capacitor creates a **lower bound** of operating frequency



CS Amplifier with Bias Circuit

- Both coupling and bypass capacitors are DC-open and AC-short

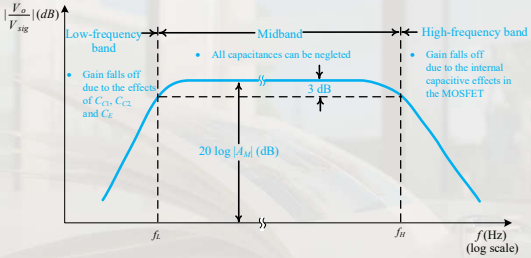
Capacitively Coupled Amplifier: DC: AC:



$$R_{in} = R_{G1} || R_{G2}$$

$$G_v = -\frac{R_{in}}{R_{in} + R_{sig}} g_m (R_D || R_L || r_o)$$

Typical Freq. Response of Capacitively Coupled Amp.



- Bandwidth

$$BW = f_H - f_L$$
$$BW \cong f_H$$

- Gain-bandwidth product

$$GB \cong |A_M|BW$$