



上海科技大学
ShanghaiTech University

EE115 Analog Circuits IC Biasing & Basic Gain Cell

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Outline



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- Building blocks of IC amplifier 1
 - IC Design Philosophy
 - IC Biasing
 - Basic Gain Cell
- Reading: SEDTRA/SMITH book pages 501-527

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IC design philosophy: **Silicon real estate**



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- Resistors are **replaced** by transistors
- Large capacitors are avoided, and small capacitors can be fabricated on chip.
- Low DC power supply voltage ($\sim 1V$)
- IC designer has the freedom to specify the device dimensions and to utilize **device matching** and arrays of devices having dimensions with specified ratios.
- Predominantly **CMOS**
 - BiCMOS provides BJT



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Discrete vs Integrated Circuits



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Discrete Circuits

- Resistors and capacitors are frequently used
- AC coupled with coupling capacitors
- High DC power supply voltage
- Transistor choice limited to available parts
- Mostly BJT, some MOS

IC

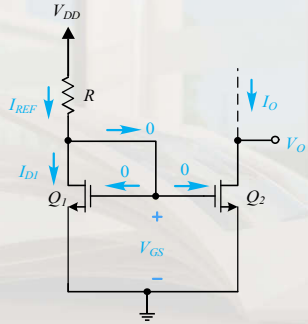
- Use mostly transistors
 - Resistors and capacitors occupy **too much areas**
- Mostly **DC coupled** (without capacitors)
- Low DC power supply voltage ($\sim 1V$)
- Can vary device size
- Predominantly CMOS
 - BiCMOS provides BJT



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Basic MOSFET Current Source

■ Neglecting channel length modulation



$$I_{D1} = \frac{1}{2} k'_n \left(\frac{W}{L} \right)_1 (V_{GS} - V_{tn})^2$$

$$I_{D1} = I_{REF} = \frac{V_{DD} - V_{GS}}{R}$$

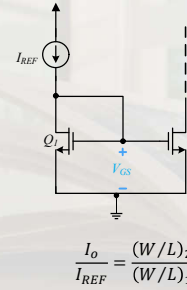
$$I_o = I_{D2} = \frac{1}{2} k'_n \left(\frac{W}{L} \right)_2 (V_{GS} - V_{tn})^2$$

$$\frac{I_o}{I_{REF}} = \frac{(W/L)_2}{(W/L)_1}$$

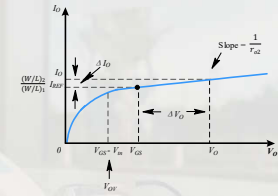
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MOS Current Source

■ Neglecting channel length modulation



■ Considering channel length modulation



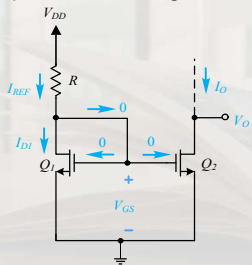
$$I_o = \frac{(W/L)_2}{(W/L)_1} I_{REF} \left(1 + \frac{V_o - V_{GS}}{V_{A2}} \right)$$

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Example: Current Source

Given $V_{DD} = 3V$ and using $I_{REF} = 100 \mu A$, design the circuit below to obtain a $100 \mu A$ nominal output current. (a) Find R if Q_1 and Q_2 are matched ($L=1\mu m$, $W=10\mu m$, $V_t=0.7V$, and $k'_n=200 \mu A/V^2$). (b) What is the lowest V_o ? (c) Assuming $V_A' = 20V/\mu m$, find R_{o2} . (d) Also, find the change in output current resulting from a $+1V$ change in V_o .

Solution:



$$I_{D1} = I_{REF} = \frac{1}{2} k'_n \left(\frac{W}{L} \right)_1 V_{OV}^2$$

$$100 = \frac{1}{2} \times 200 \times 10 V_{OV}^2$$

$$V_{OV} = 0.316V$$

$$V_{GS} = V_t + V_{OV} = 0.7 + 0.316 \approx 1V$$

$$R = \frac{V_{DD} - V_{GS}}{I_{REF}} = \frac{3V - 1V}{0.1mA} = 20k\Omega$$

$$V_{omin} = V_{OV} \approx 0.3V$$

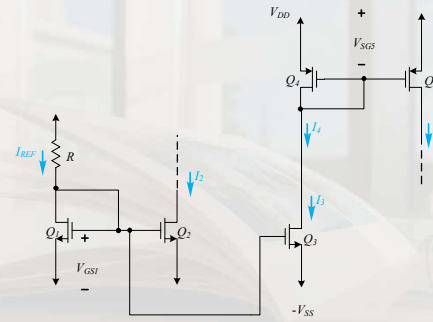
$$V_A = 20 \times 1 = 20V$$

$$R_{o2} = r_{o2} = \frac{20V}{100\mu A} = 0.2M\Omega$$

$$\Delta I_o = \frac{\Delta V_o}{r_{o2}} = \frac{1V}{0.2M\Omega} = 5\mu A$$

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MOS Current Steering Circuits



$$I_2 = I_{REF} \frac{(W/L)_2}{(W/L)_1}$$

$$I_3 = I_{REF} \frac{(W/L)_3}{(W/L)_1}$$

$$I_4 = I_3$$

$$I_5 = I_4 \frac{(W/L)_5}{(W/L)_4}$$

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Review: MOSFET r_o and g_m

Output resistance at drain:

$$r_o = \frac{V_A}{I_D} = \frac{V'_A L}{I_D}$$

Transconductance:

$$i_D = I_D + i_d = \frac{1}{2} k_n (V_{GS} + v_{gs} - V_{tn})^2$$

$$= \frac{1}{2} k_n (V_{GS} - V_{tn})^2 + k_n (V_{GS} - V_{tn}) v_{gs} + \frac{1}{2} k_n v_{gs}^2$$

$$i_d = k_n (V_{GS} - V_{tn}) v_{gs}$$

Or

Or

$$g_m = k_n V_{OV} = k'_n (W/L) V_{OV}$$

Or

$$g_m = \frac{2I_D}{V_{GS} - V_{tn}} = \frac{2I_D}{V_{OV}} = \frac{I_D}{V_{OV}/2}$$

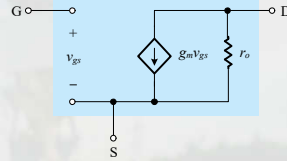
Three design parameters: W/L , V_{OV} , and I_D .

$$g_m \equiv \frac{\partial i_D}{\partial v_{gs}} \bigg|_{v_{gs}=V_{GS}}$$

$$g_m = \frac{i_d}{v_{gs}} = k_n (V_{GS} - V_{tn}) = k_n V_{OV}$$

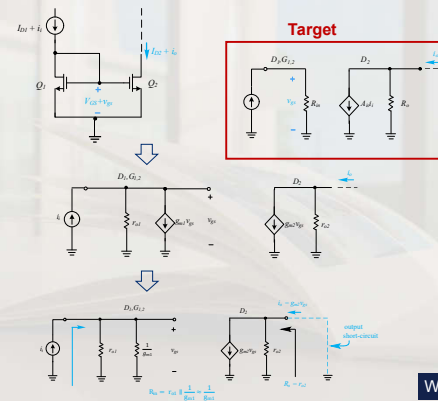
$$V_{OV} = \sqrt{2I_D/k_n} = \sqrt{2I_D/(k'_n W/L)}$$

$$g_m = \sqrt{2k'_n W/L} \sqrt{I_D}$$



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Small-Signal Analysis



$$R_{in} = r_{o1} \parallel \frac{1}{g_{m1}} \cong \frac{1}{g_{m1}}$$

$$R_o = r_{o2}$$

$$A_{is} \equiv \frac{i_o}{i_i} \bigg|_{v_{d2}=0} = \frac{g_{m2} v_{gs}}{i_i}$$

$$v_{gs} = i_i R_{in} = \frac{i_i}{g_{m1} + \frac{1}{r_{o1}}}$$

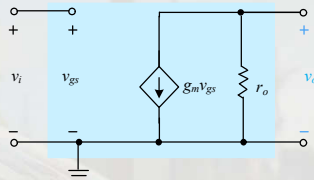
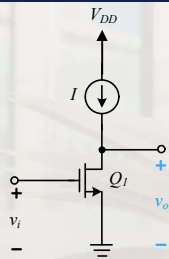
$$A_{is} = \frac{g_{m2}}{g_{m1} + \frac{1}{r_{o1}}}$$

$$A_{is} = \frac{(W/L)_2}{(W/L)_1} \frac{1}{1 + 1/(g_{m1} r_{o1})}$$

Why current mirror is an excellent current amplifier? 0/16

CS Cell w/ Ideal Current Source Load

Ideal Current Source Load



$$R_{in} = \infty$$

$$A_{vo} = -g_m r_o$$

$$R_o = r_o$$

■ Intrinsic gain

$$g_m = \frac{I_D}{V_{OV}/2}$$

$$r_o = \frac{V_A}{I_D} = \frac{V'_A L}{I_D}$$

$$A_o = g_m r_o = \frac{V_A}{V_{OV}/2} = \frac{V'_A L}{V_{OV}/2}$$

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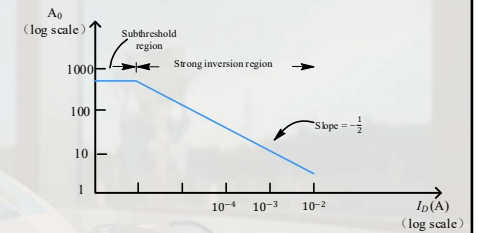
Intrinsic Gain $g_m r_o$

■ MOSFET

$$g_m = \sqrt{2\mu_n C_{ox} (W/L) I_D}$$

$$r_o = \frac{V_A}{I_D} = \frac{V'_A L}{I_D}$$

$$A_o = g_m r_o = \frac{V'_A \sqrt{2(\mu_n C_{ox}) (WL)}}{\sqrt{I_D}}$$

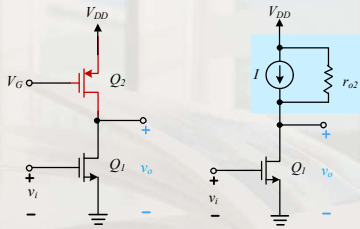


Smaller current gives higher intrinsic gain, but paid by smaller g_m and bandwidth.

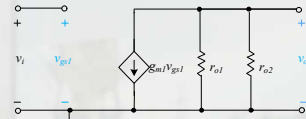
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Output Resistance of Current Source Load

Current source loaded/active loaded



$$I = \frac{1}{2} (\mu_p C_{ox}) \left(\frac{W}{L} \right)_2 [V_{DD} - V_G - |V_{tp}|]^2$$



$$r_{o2} = \frac{|V_{A2}|}{I}$$

$$A_v \equiv \frac{v_o}{v_i} = -g_{m1}(r_{o1} || r_{o2})$$

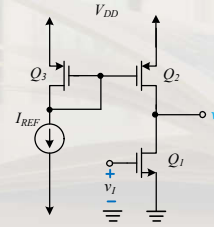
$$A_v = -\frac{1}{2} g_m r_o$$

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Example: CS amplifier with current-source load

- Given a common source amplifier with current source load. Assume that Q_2 and Q_3 are matched. Let $V_{DD}=1.8$ V, $V_{tn}=-V_{tp}=0.5$ V, $\mu_n C_{ox}=400 \mu\text{A}/\text{V}^2$, $\mu_p C_{ox}=100 \mu\text{A}/\text{V}^2$, $|V_A|=5$ V for all transistors, and $I_{REF}=100 \mu\text{A}$.

- (a) Find the dc component of v_o and W/L so that all transistors operate at $|V_{OV}|=0.2$ V.



Solution (a)

$$V_{GS1} = V_{tn} + V_{OV} = 0.5 + 0.2 = 0.7\text{ V}$$

$$V_1 = V_{GS1} = 0.7\text{ V}$$

$$I_{D1} = \frac{1}{2} (\mu_n C_{ox}) \left(\frac{W}{L} \right)_1 V_{OV}^2$$

$$100 = \frac{1}{2} \times 400 \times \left(\frac{W}{L} \right)_1 \times 0.2^2$$

$$\Rightarrow \left(\frac{W}{L} \right)_1 = 12.5$$

$$V_{GS1} = V_{tn} + V_{OV} = 0.5 + 0.2 = 0.7\text{ V}$$

$$I_{D2,3} = \frac{1}{2} (\mu_p C_{ox}) \left(\frac{W}{L} \right)_{2,3} V_{OV}^2$$

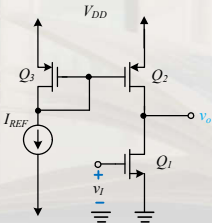
$$100 = \frac{1}{2} \times 100 \times \left(\frac{W}{L} \right)_{2,3} \times 0.2^2$$

$$\Rightarrow \left(\frac{W}{L} \right)_{2,3} = 50$$

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Example: CS amplifier with current-source load

- $V_{DD}=1.8$ V, $V_{tn}=-V_{tp}=0.5$ V, $\mu_n C_{ox}=400 \mu\text{A}/\text{V}^2$, $\mu_p C_{ox}=100 \mu\text{A}/\text{V}^2$, $|V_A|=5$ V for all transistors, and $I_{REF}=100 \mu\text{A}$.
- (b) Determine the small-signal voltage gain.
- (c) What is the allowable range of signal swing at the output for almost-linear operation?



Solution (b)

$$g_{m1} = \frac{2I_{D1}}{V_{OV1}} = \frac{2 \times 0.1\text{ mA}}{0.2\text{ V}} = 1\text{ mA/V}$$

$$r_{o1} = \frac{V_{A1}}{I_{D1}} = \frac{5\text{ V}}{0.1\text{ mA}} = 50\text{ k}\Omega$$

$$r_{o2} = \frac{|V_{A2}|}{I_{D2}} = \frac{5\text{ V}}{0.1\text{ mA}} = 50\text{ k}\Omega$$

$$A_v = -g_{m1}(r_{o1} || r_{o2})$$

$$= -1(50 || 50)$$

$$= -25\text{ V/V}$$

Solution (c)

$$v_{Omax} = 1.8 - 0.2 = 1.6\text{ V}$$

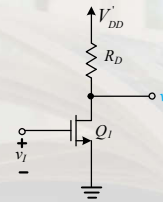
$$v_{Omin} = 0.2\text{ V}$$

$$0.2\text{ V} \leq v_o \leq 1.6\text{ V}$$

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Example: CS amplifier with current-source load

- $V_{DD}=1.8$ V, $V_{tn}=-V_{tp}=0.5$ V, $\mu_n C_{ox}=400 \mu\text{A}/\text{V}^2$, $\mu_p C_{ox}=100 \mu\text{A}/\text{V}^2$, $|V_A|=5$ V for all transistors, and $I_{REF}=100 \mu\text{A}$.
- (d) If the current-source load is replaced with a resistance R_D connected to V_{DD} as shown below, find R_D and V_{DD}' to keep I_D the voltage gain, and the output signal swing unchanged.



Solution (d)

$$0.2\text{ V} \leq v_o \leq 1.6\text{ V}$$

$$R_D = r_{o2} = 50\text{ k}\Omega$$

Bias Q_1 to make V_{DS1} equal to the middle point, so that the output swing unchanged.

$$V_{DS1} = 0.9\text{ V}$$

$$V_{DD}' = V_{DS1} + I_D R_D$$

$$= 0.9 + 0.1 \times 50 = 5.9\text{ V}$$

Why current source load is better?

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