

EE115 Analog Circuits

Diff Amp: CMRR, offset, current mirror load

Prof. Haoyu Wang
Office: SIST Bldg. 3-530
wanghy@shanghaitech.edu.cn



PEARL
电力电子与再生能源实验室

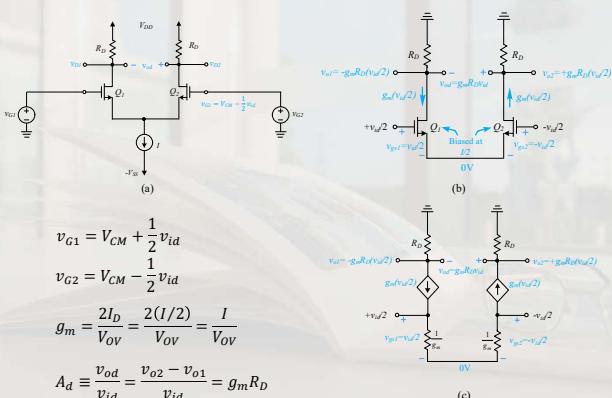
Outline

- Differential amplifiers 2
 - Common-Mode Rejection
 - DC Offset
 - Differential Amplifier with Current Mirror Load
- Reading: SEDTRA/SMITH book pages 609-639

2/17

PEARL
电力电子与再生能源实验室

Review: Small Signal Operation



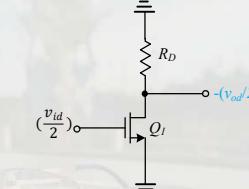
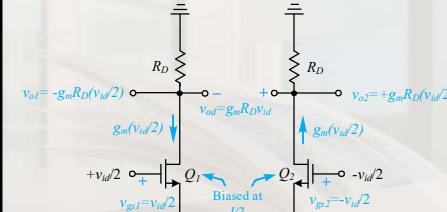
■ For **differential AC small signal**, the differential pair is **anti-symmetric**. The potential at the mid point is zero. This is called **Virtual Ground**

■ This virtual ground is obtained **without bypass capacitor**
-> much smaller area and better frequency response

3/17

Review: Differential Half Circuit

- Because the two halves of the circuits are **anti-symmetric**, and **source is at virtual ground**, we can simplify and just analyze the **half circuit**

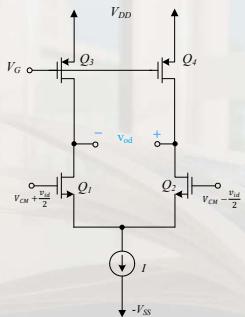


$$A_d = g_m (R_D || r_o)$$

4/17

PEARL
电力电子与再生能源实验室

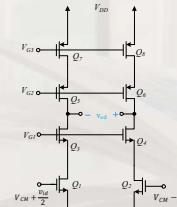
Review: Diff. Amplifier w/ Current-Source Loads



$$A_d \equiv \frac{v_{od}}{v_{id}} = g_{m1}(r_{o1} || r_{o3})$$

Review: Cascode Differential Amplifier

- Cascode configurations for both amplifying transistors and current source loads.



(a)



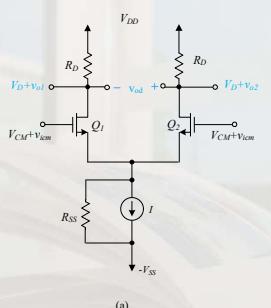
(b)

$$A_d \equiv \frac{v_{od}}{v_{id}} = g_{m1}(R_{on} || R_{op})$$

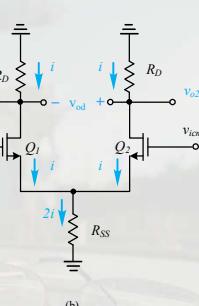
$$R_{on} = (g_{m3}r_{o3})r_{o1}$$

$$R_{op} \equiv (g_{m5}r_{o5})r_{o7}$$

AC Equivalent Circuit for Common Mode Input



(a)

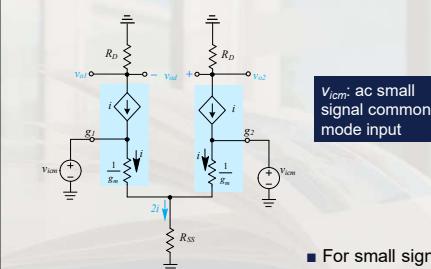


(b)

- Non-ideal current source consists of an ideal current source, shunted by a large resistance, R_{ss} .

Common Mode Half Circuit

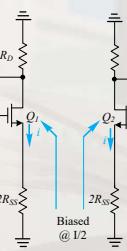
- For differential inputs, the two half circuits are anti-symmetric, and the joint (Source) is always at virtual ground.



- For small signal common-mode inputs, the two half circuits are symmetric. The Source is not virtual ground any more.
- R_{ss} can be considered as two parallel $2R_{ss}$.
- Each CM half circuit has $2R_{ss}$ connected to the source.

Ideal CM Output Voltage

Common-Source with degeneration



$$v_{icm} = \frac{i}{g_m} + 2iR_{SS}$$

$$i = \frac{v_{icm}}{1/g_m + 2R_{SS}}$$

$$v_{o1} = v_{o2} = -\frac{R_D}{1/g_m + 2R_{SS}} v_{icm}$$

$$\frac{v_{o1}}{v_{icm}} = \frac{v_{o2}}{v_{icm}} \cong -\frac{R_D}{2R_{SS}}$$

$$v_{od} = v_{o1} - v_{o2} = 0$$

- v_{od} is 0 for **ideal** diff pair
 - 1. Perfectly matched transistors and resistors.
 - 2. Small CM voltage to keep Q_1 & Q_2 in saturation.

9/17

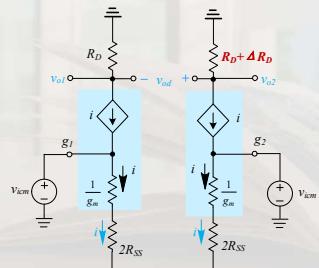


电力电子与再生能源实验室

Common Mode Gain with Mismatched R_D

- However, any **mismatch** in the half circuits will produce **finite output voltage**.

Case 1: R_D mismatch



$$v_{o1} \cong -\frac{R_D}{2R_{SS}} v_{icm}$$

$$v_{o2} \cong -\frac{R_D + \Delta R_D}{2R_{SS}} v_{icm}$$

$$v_{od} = v_{o1} - v_{o2} = -\frac{\Delta R_D}{2R_{SS}} v_{icm}$$

$$A_{cm} \equiv \frac{v_{od}}{v_{icm}} = -\frac{\Delta R_D}{2R_{SS}} = -\left(\frac{R_D}{2R_{SS}}\right)\left(\frac{\Delta R_D}{R_D}\right)$$

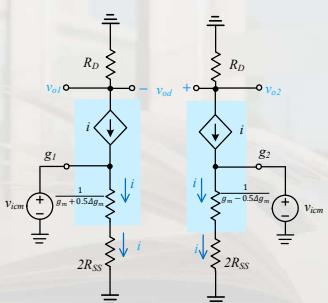
$$\text{CMRR}(dB) = 20 \log \frac{|A_d|}{|A_{cm}|}$$

$$\text{Since } A_d = g_m R_{SS}, \quad \text{CMRR} = (2g_m R_{SS}) / \left(\frac{\Delta R_D}{R_D}\right)$$

10/17

Common Mode Gain with Mismatched g_m

Case 2: g_m mismatch



$$g_{m1} = g_m + \frac{1}{2}\Delta g_m$$

$$g_{m2} = g_m - \frac{1}{2}\Delta g_m$$

$$g_{m1} - g_{m2} = \Delta g_m$$

$$A_{cm} \cong \left(\frac{R_D}{2R_{SS}}\right) \left(\frac{\Delta g_m}{g_m}\right)$$

$$\text{CMRR} = (2g_m R_{SS}) / \left(\frac{\Delta g_m}{g_m}\right)$$

11/17



电力电子与再生能源实验室

Example-CMRR of MOS differential pair

- Design a MOS diff pair with 100 dB CMRR. The only source of mismatch is a 2% mismatch in Q_1 and Q_2 's W/L ratios. Let $I = 200\mu A$ and assume that all transistors have $V_{OV} = 0.2V$. $V_A' = 5A/\mu m$.
- a) If a **simple current source** is used for I , what channel length is needed?

Solution:

Mismatch of W/L ratios leads to mismatch of g_m

$$g_m = (\mu_n C_{ox}) \left(\frac{W}{L}\right) V_{OV}$$

$$\text{CMRR} = (2g_m R_{SS}) / \left(\frac{\Delta g_m}{g_m}\right)$$

$$100dB = 10^5 = \frac{(2g_m R_{SS})}{0.02} *$$

$$g_m = \frac{2I_D}{V_{OV}} = \frac{2 \times (I/2)}{V_{OV}} = \frac{2 \times 0.1}{0.2} = 1mA/V$$

$$V_A = V_A' L = 5L \rightarrow L = 40\mu m$$

Substituting into *,

$$R_{SS} = 1M\Omega$$

For a **simple current source**

$$r_o = R_{SS} = 1M\Omega$$

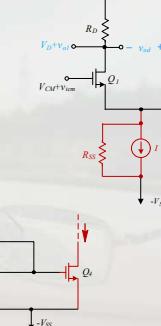
$$r_o = \frac{V_A}{I} = 1M\Omega$$

$$\text{Since } I = 200\mu A$$

$$V_A = 200V$$

$$I_{REF} = I_D = 200\mu A$$

Too large!



12/36

Example-continued

➤ b) If a cascode current source is used for I , what channel length is needed?

Solution:

For a cascode current source

$$R_{SS} = (g_m r_o) r_o = 1M\Omega$$

$$g_m = \frac{2I}{V_{OV}} = \frac{2 \times 0.2}{0.2} = 2mA/V$$

Thus $1M\Omega = 2mA/V \times r_o^2$

$$r_o = 22.36k\Omega$$

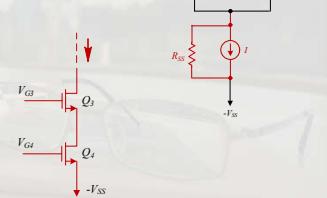
$$r_o = 22.36k\Omega = \frac{V_A}{I} = \frac{V_A}{0.2}$$

$$V_A = 4.47V = V_A L = 5L$$

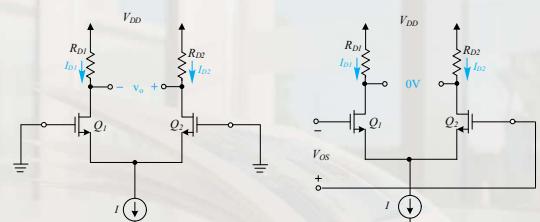
$$L = 0.89\mu m$$

A considerable reduction of chip area!

13/36



DC Offset



$$A_d \equiv \frac{v_{od}}{v_{id}} = \frac{v_{o2} - v_{o1}}{v_{id}} = g_m R_D$$

$$R_{D1} = R_D + \frac{\Delta R_D}{2}$$

$$R_{D2} = R_D - \frac{\Delta R_D}{2}$$

$$V_{D1} = V_{DD} - \frac{I}{2} \left(R_D + \frac{\Delta R_D}{2} \right)$$

$$V_{D2} = V_{DD} - \frac{I}{2} \left(R_D - \frac{\Delta R_D}{2} \right)$$

$$V_O = V_{D2} - V_{D1} = \left(\frac{I}{2} \right) \Delta R_D$$

$$V_{OS} = \left(\frac{V_{OV}}{2} \right) \left(\frac{\Delta R_D}{R_D} \right)$$

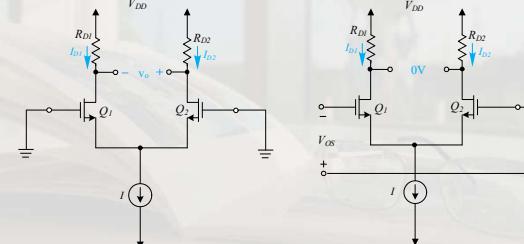
$$g_m = \frac{I}{V_{OV}/2} = \frac{I}{V_{OV}}$$

15/17

DC Offset

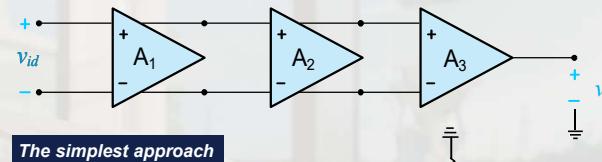
■ Due to mismatch in R_D , $V_O \neq 0$ even when both inputs are grounded.

■ To produce 0 output, an **input offset voltage** $V_{OS} = V_O/A_d$ needs to be applied. A_d is differential gain

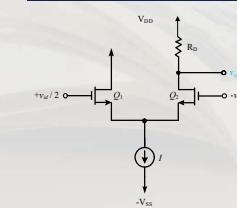


14/17

Differential-to-Single-Ended Conversion



The simplest approach



Simple but inefficient: the current signal in Q_1 is not utilized, leading to loss of a factor of 2 in gain.

16/17

Differential Pair w/ Current Mirror Load

A much better approach

