上海科技大学
ShanghaiTech University

EE115 Analog Circuits
MOSFET

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PEARL 电力电子与再生能源实验室

Outline

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- MOSFET
  - ➢ Device Structure and Physical Operation
  - ➢ Current-Voltage Characteristics
  - ➢ MOSFET Circuits at DC
- Reading: SEDTRA/SMITH book pages 244-284

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MOSFET

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- MOSFET: metal-oxide-semiconductor field effect transistor
- Typically
  - ➢ Channel length: L ~ 20 nm to 1 μm
  - ➢ Channel width: W ~ 30 nm to 100 μm
  - ➢ Oxide thickness: t_{ox} ~ 1 to 10 nm

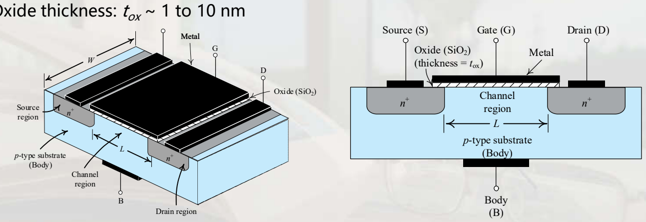

Fig. Physical structure of the enhancement-type NMOS transistor: **(a)** perspective view; **(b)** cross section

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NMOSFET (NMOS)

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- **N-channel** MOSFET
  - ➢ Current conducted by e-s
- 3 terminal device
  - ➢ **Source (S)**: n+ (heavily doped n-type)
  - ➢ **Drain (D)**: n+
  - ➢ **Gate (G):** metal deposited on insulator above channel
- **Substrate (Body)** is a 4th terminal
  - ➢ Substrate is p-doped
- Electrons are induced in channel when a positive gate voltage is applied
- Electrons moves from Source to Drain
  - ➢ Current flows from D to S

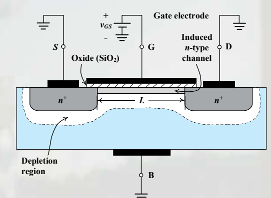


Fig. Enhancement-type NMOS transistor with a positive voltage applied to the gate. An n channel is induced at the top of the substrate beneath the gate.

Why n channel is called inversion layer?

Creating a Channel for Current Flow

- MOS is a capacitor across an insulator (oxide). When a positive voltage is applied at Gate, electrons are induced under the gate.
- At **threshold**, sufficient number of electrons form a **channel** between Source and Drain, forming a conductive channel.
- Total charge in the channel:

  $|Q| = C_{ox} \cdot WL(v_{GS} - V_t)$

  where $C_{ox} = \varepsilon_{ox}/t_{ox}$ is oxide capacitance per unit area
  - $\varepsilon_{ox} = 3.9\varepsilon_0 = 3.9 \times 8.854 \times 10^{-12}$ F/m
  - W: gate width
  - L : gate length
  - V_t : Threshold voltage
  - $v_{GS} - V_t \equiv v_{OV}$ is called **Overdrive Voltage**

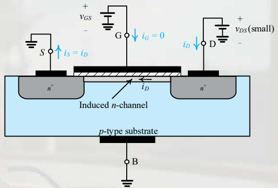


Fig. NMOS with $v_{GS} > V_t$ and with a small v_{DS}

Current at Small v_{DS}

- When $v_{OV} = v_{GS} - V_t > 0$, a channel is formed between Source and Drain.
- Charge per unit channel length:

$$\text{charge density} = \frac{|Q|}{L} = C_{ox} W v_{ov}$$

- Electric field along the channel:

$$|E| = \frac{v_{DS}}{L}$$

- Drain current = charge density × electron drift velocity:

$$i_D = (C_{ox} W v_{ov})\left(\mu_n \frac{v_{DS}}{L}\right) = \left[\mu_n C_{ox} \frac{W}{L} v_{ov}\right] v_{DS}$$

- At small v_{DS}, the transistor behaves like a gate-controlled **variable resistor**

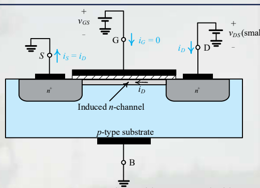


Fig. An NMOS transistor with $v_{GS} > V_t$ and with a small v_{DS} applied.

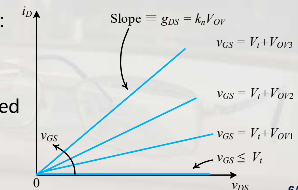


Fig. i_D - v_{DS} characteristics of the MOSFET, when v_{DS} is kept small.

Continued

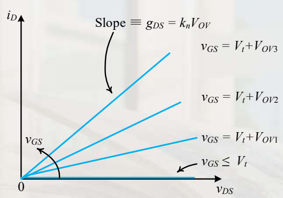


Fig. i_D - v_{DS} characteristics of the MOSFET in Fig. 5.3 when the voltage applied between drain and source, v_{DS}, is kept small.

- Transconductance parameters:

$$k_n' = \mu_n C_{ox}$$

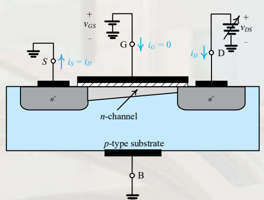
$$k_n = k_n'(W/L) = \mu_n C_{ox}(W/L)$$

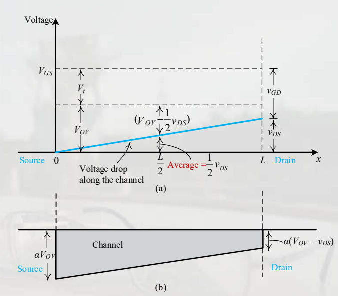
- Gate-controlled resistance

$$r_{DS} = \frac{1}{\mu_n C_{ox}(W/L)(v_{GS} - V_t)}$$

Triode Region ($v_{DS} < v_{OV}$)

- As v_{DS} increases, the potential in the channel is no longer a constant.
- Assume the channel potential is $v(x)$:





$$i_D = k_n' \frac{W}{L}\left(V_{OV} - \frac{1}{2} v_{DS}\right) v_{DS} = k_n' \frac{W}{L}\left[(v_{GS} - V_t) v_{DS} - \frac{1}{2} v_{DS}^2\right]$$

I-V curve

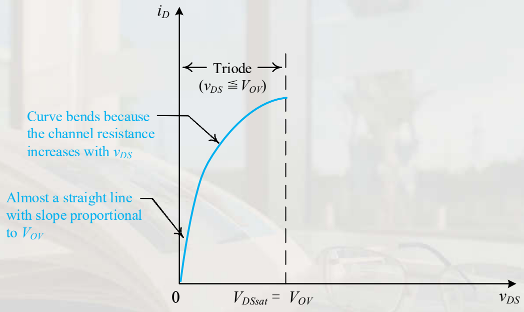
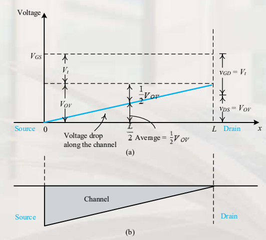


Fig. i_D versus v_{DS} for an enhancement-type NMOS transistor operated with $v_{GS} = V_t + V_{OV}$

Pinch-Off (v_{DS}=v_{OV})



- The channel potential at the drain side is v_{DS}.
- When v_{DS}=v_{OV}, the local charge density at the drain becomes zero.
- So the channel is **pinched off** near the Drain.
- Once the channel is **pinched off,** the drain current remains **constant**:

$$i_D = \frac{1}{2} k_n' \frac{W}{L} V_{OV}^2$$

- This region, v_{DS}>v_{OV} , is called **Saturation**

$$v_{DSsat} = v_{OV} = v_{GS} - V_t$$

$$i_D = \frac{1}{2} k_n' \frac{W}{L} (v_{GS} - V_t)^2$$

Saturation Region (v_{DS}>v_{OV})

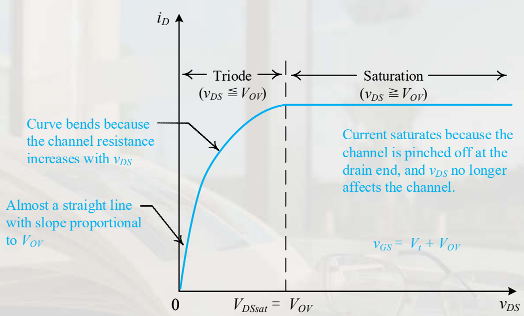
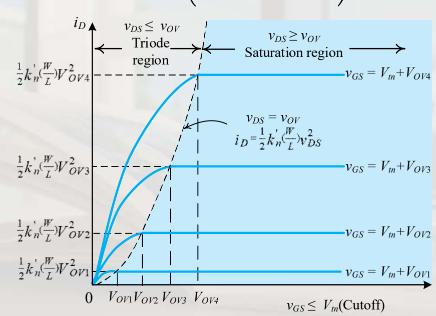


Fig. i_D versus v_{DS} for an enhancement-type NMOS transistor operated with $v_{GS} = V_t + V_{OV}$

I-V Curves of NMOS

$$i_D = k_n' \frac{W}{L}\left(V_{OV} v_{DS} - \frac{1}{2} v_{DS}^2\right)$$

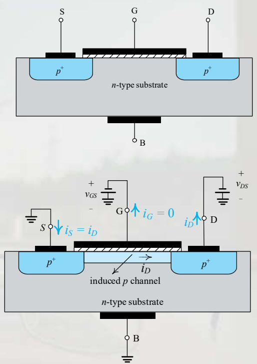


$$i_D = \frac{1}{2} k_n' \frac{W}{L} V_{OV}^2$$

Fig. i_D - v_{DS} characteristic for an enhancement-type NMOS transistor.

PMOSFET (PMOS)

- P-channel MOSFET
  - Current conducted by holes
- 3 terminal device
  - **Source (S)**: p+ (heavily p-type)
  - **Drain (D):** p+
  - **Gate (G)**: metal deposited on insulator above channel
- Substrate (called **Body**) is a 4^{th} terminal
  - Substrate is n-doped
- **Holes** is induced in channel when a **negative** gate voltage is applied
- Holes moves from Source to Drain
  - Current flows from S to D



CMOS (Complementary MOS)

- CMOS is the prevalent IC technology today
- Since NMOS and PMOS are formed on oppositely doped substrates, one of the transistor needs to be placed in a **well**
- PMOS is placed in an **n well** here.
- Alternatively, NMOS can be placed in p well

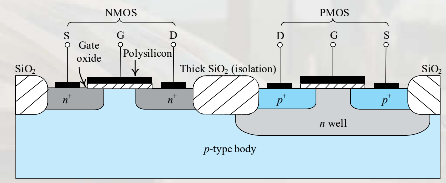
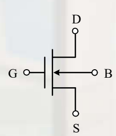
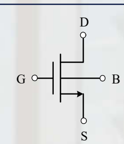


Fig. Cross section of a CMOS integrated circuit.

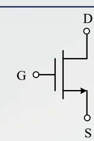
Circuit Symbol for NMOS



(a)



(b)



(c)

- 4 terminal including
  - Body (Arrow pointing **to** channel indicating
  - substrate is **p-type**
- Modified circuit symbol with arrow on source (Arrow indicating direction of current flow)
- Simplified circuit symbol with body connected to source (or when body effect is unimportant)

- Note in NMOS
  - **Drain voltage > Source voltage**
  - Current always flows from **Drain to Source**

Relative Voltage Levels of NMOS

- **V_{tn}: threshold voltage of NMOS**
- V_{tn} is usually fixed once a **process (technology)** is selected

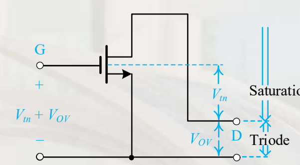


Fig. The relative levels of the terminal voltages of the enhancement NMOS transistor for operation in the triode region and in the saturation region.

Analog Circuit (e.g., linear amplifiers) usually biased in Saturation region

Digital circuit (e.g. inverter) and power electronics (switch mode power supply) use Triode region as one of the states

Drain Current vs Gate Voltage

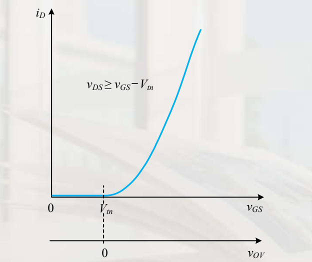


Fig. i_D-v_{GS} characteristic of an NMOS transistor operating in the saturation region.

- In Saturation Region

$$i_D = \frac{1}{2} k_n' \frac{W}{L} (v_{GS} - V_{tn})^2$$

- To experimentally determine V_{tn}:

$$\sqrt{i_D} \propto (v_{GS} - V_{tn})$$

Finite r_o due to Channel length Modulation

- When $v_{DS} = v_{OV}$
  - **Pinch-off** happens
- When $v_{DS} > v_{OV}$
  - Pinch-off point **shifts** to the source

$$i_D = \frac{1}{2} k_n' \frac{W}{L} (v_{GS} - V_{tn})^2 (1 + \lambda v_{DS})$$

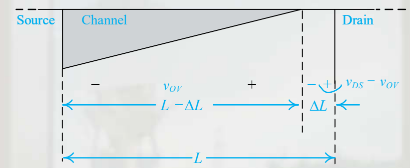


Fig. Increasing v_{DS} beyond v_{DSsat} causes the channel pinch-off point to move slightly away from the drain, thus reducing the effective channel length (by ΔL)

Output Resistance of MOSFET

- Early Voltage
  - V_A early voltage, $V_A = \frac{1}{\lambda}$
  - V_A' early voltage/length, process dependent

$$V_A = V_A' L$$

- Output resistance of NMOS:

$$r_o \equiv \left[\frac{\partial i_D}{\partial v_{DS}}\right]^{-1}_{v_{GS}\ \text{constant}} = \left[\lambda \frac{1}{2} k_n' \frac{W}{L} (v_{GS} - V_{tn})^2\right]^{-1} = \frac{1}{\lambda I_D}$$

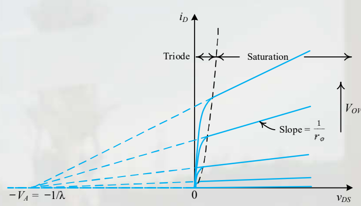
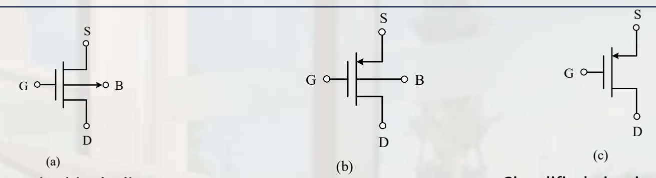


Fig. Effect of v_{DS} on i_D in the saturation region.

Due to CLM, the output resistance of MOSFET is not infinite, but still a large value at least for long-channel device.

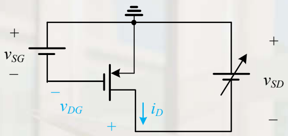
Circuit Symbol of PMOS

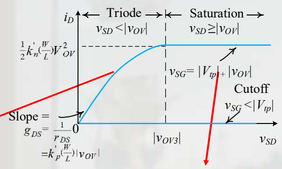


- 4 terminal including Body (Arrow pointing **from** channel indicating substrate is **n-type**
- Modified circuit symbol with arrow on source (Arrow indicating **direction of current flow**)
- Simplified circuit symbol with body connected to source (or when the effect of the body on device operation is unimportant)

- Note in PMOS
  - **Source voltage > Drain voltage**
  - Current always flows from **Source to Drain**
  - **Source** is usually drawn on **top** so current flows downward (convention)

PMOS I-V Equations





■ Triode Region

$$i_D = k_p' \frac{W}{L}\left(|v_{OV}| - \frac{1}{2}v_{SD}\right)v_{SD}$$

■ Saturation Region

$$i_D = \frac{1}{2}k_p' \frac{W}{L}|v_{OV}|^2 = \frac{1}{2}k_p' \frac{W}{L}v_{OV}^2$$

Relative Voltage Levels of PMOS

- **V_{tp}: threshold voltage of PMOS**
- V_{tp} is usually fixed once a **process (technology)** is selected

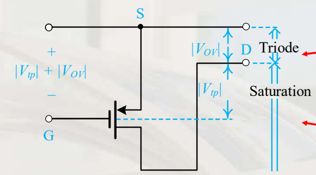


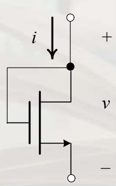
Fig. The relative levels of the terminal voltages of the enhancement-type PMOS transistor for operation in the triode region and in the saturation region.

Digital circuit (e.g. inverter) and power electronics (switch mode power supply) use Triode region as one of the states

Analog Circuit (e.g., linear amplifiers) usually biased in Saturation region

Diode-Connected Transistor

- With Gate connected to Drain, it becomes a 2-terminal device.
- This is called ***diode-connected*** transistor.
- In this configuration, the transistor is always in Saturation.



$$i_D = \frac{1}{2}k_n' \frac{W}{L}(v_{GS} - V_{tn})^2$$

Now $i = i_D$, and $v = v_{GS}$, thus

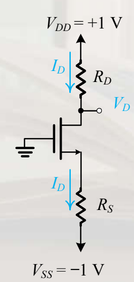
$$i = \frac{1}{2}k_n' \frac{W}{L}(v - V_{tn})^2$$

Replacing $k_n' W/L$ by k_n results in

$$i = \frac{1}{2}k_n(v - V_{tn})^2$$

Design problem:

Determine R_S and R_D such that the NMOS is biased at I_D = 0.2mA and V_D = 0.2V. The NMOS has V_{tn} = 0.5V, $\mu_n C_{ox}$ =400 μA /V², L =0.5 μm and W = 15 μm. λ=0.



Solution:

$$R_D = \frac{V_{DD} - V_D}{I_D} = \frac{1 - 0.2}{0.2} = 4\ k\Omega$$

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}V_{OV}^2$$

$$200 = \frac{1}{2} \times 400 \times \frac{15}{0.5}V_{OV}^2$$

$$V_{OV} = 0.18\ \text{V}$$

$$V_{GS} = V_t + V_{OV} = 0.5 + 0.18 = 0.68\ \text{V}$$

$$R_S = \frac{V_S - V_{SS}}{I_D} = \frac{-0.68 - (-1)}{0.2} = 1.6\ k\Omega$$