



上海科技大学
ShanghaiTech University

EE115 Analog Circuits Transistor Amplifier 1

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Outline



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■ Transistor Amplifier 1

- MOSFET Review
- Basic Principles
- Small-Signal Operation and Models

■ Reading: SEDTRA/SMITH book pages 367-393

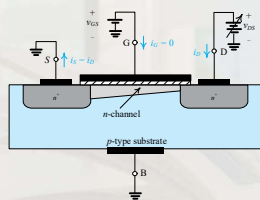
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Review: Triode Region ($v_{DS} < v_{OV}$)

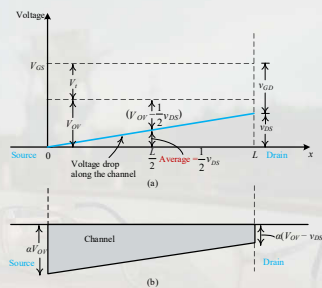


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- As v_{DS} **increases**, the potential in the channel is **no longer** a constant.
- Assume the channel potential is $v(x)$:



$$i_D = k'_n \frac{W}{L} \left(V_{OV} - \frac{1}{2} v_{DS} \right) v_{DS} = k'_n \frac{W}{L} \left[(v_{GS} - V_t) v_{DS} - \frac{1}{2} v_{DS}^2 \right]$$



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Review: Pinch-Off ($v_{DS} = v_{OV}$)



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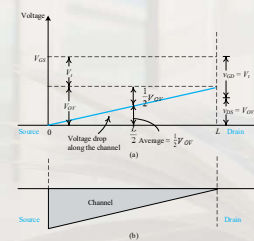
- The channel potential at the drain side is v_{DS} .
- When $v_{DS} = v_{OV}$, the local charge density at the drain becomes zero.
- So the channel is **pinched off** near the Drain.
- Once the channel is **pinched off**, the drain current remains **constant**:

$$i_D = \frac{1}{2} k'_n \frac{W}{L} V_{OV}^2$$

- This region, $v_{DS} > v_{OV}$, is called **Saturation**

$$v_{DSSat} = v_{OV} = v_{GS} - V_t$$

$$i_D = \frac{1}{2} k'_n \frac{W}{L} (v_{GS} - V_t)^2$$



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Review: I-V Curves of NMOS

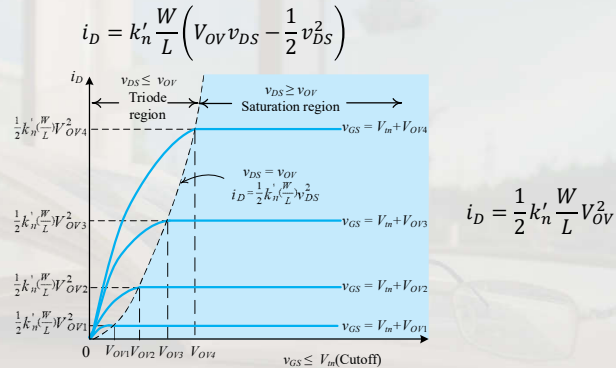
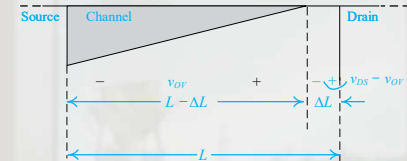


Fig. $i_D - v_{DS}$ characteristic for an enhancement-type NMOS transistor.

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Review: Finite r_o due to Channel length Modulation

- When $v_{DS} = v_{OV}$
 - Pinch-off happens



- When $v_{DS} > v_{OV}$
 - Pinch-off point **shifts** to the source
- $$i_D = \frac{1}{2} k'_n \frac{W}{L} (v_{GS} - V_{tn})^2 (1 + \lambda v_{DS})$$

Fig. Increasing v_{DS} beyond v_{DSsat} causes the channel pinch-off point to move slightly away from the drain, thus reducing the effective channel length (by ΔL).

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Review: Output Resistance of MOSFET

- Output resistance of NMOS:

$$r_o \equiv \left[\frac{\partial i_D}{\partial v_{DS}} \right]_{v_{GS} \text{ constant}}^{-1} = \left[\lambda \frac{1}{2} k'_n \frac{W}{L} (v_{GS} - V_{tn})^2 \right]^{-1} = \frac{1}{\lambda I_D}$$

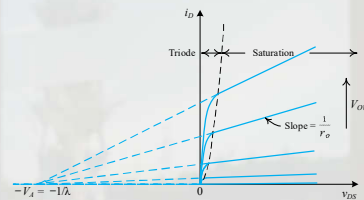


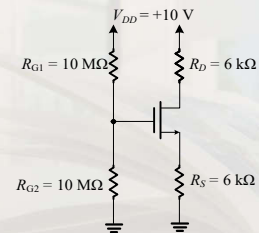
Fig. Effect of v_{DS} on i_D in the saturation region.

Due to CLM, the output resistance of MOSFET is not infinite, but still a large value at least for long-channel device.

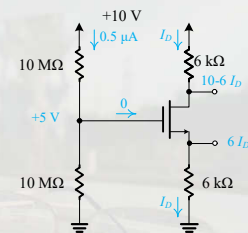
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DC operating point:

Analyze the circuit to determine the voltages at all nodes and the currents through all branches. Let $V_{tn} = 1 \text{ V}$ and $k'_n (W/L) = 1 \text{ mA/V}^2$, $\lambda = 0$.

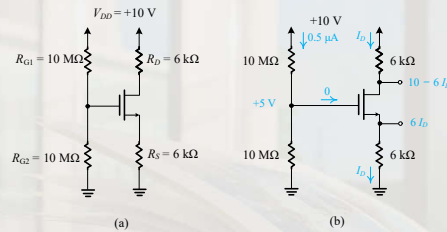


Solution:



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Solution



$$V_G = V_{DD} \frac{R_{G2}}{R_{G2} + R_{G1}} = 10 \times \frac{10}{10 + 10} = +5 \text{ V}$$

Assume **saturation**

$$V_{GS} = 5 - 6I_D$$

$$I_D = \frac{1}{2} k_n' \frac{W}{L} (V_{GS} - V_{tn})^2 = \frac{1}{2} \times 1 \times (5 - 6I_D - 1)^2$$

$$18I_D^2 - 25I_D + 8 = 0$$

$$I_D = 0.5 \text{ mA}$$

$I_D = 0.89 \text{ mA}$ **Abandon**

$$V_S = 0.5 \times 6 = +3 \text{ V}$$

$$V_{GS} = 5 - 3 = 2 \text{ V}$$

$$V_D = 10 - 6 \times 0.5 = +7 \text{ V}$$

Assumption validated!

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Transistor Operating Mode in Amplifiers

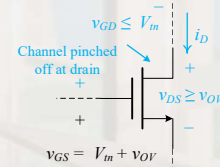
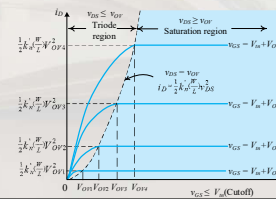


Fig. NMOS in the saturation region



- Transistors are biased in **flat** part of the I-V curves

➤ **Saturation** mode for MOSFET

- Channel **pinched off** at drain

➤ Drain voltage can vary without changing current

$$i_D = \frac{1}{2} k_n (v_{GS} - V_{tn})^2$$

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Voltage Transfer Curves

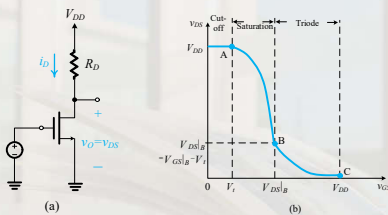


Fig. An NMOS amplifier and (b) its VTC

- Transistors are **transconductance** amplifiers

➤ MOSFET: v_{GS} controls i_D

- Adding load resistors **converts** current to voltage → voltage amplifiers

➤ Drain voltage free to change in saturation mode

$$v_{DS} = V_{DD} - i_D R_D$$

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Biasing the amplifier

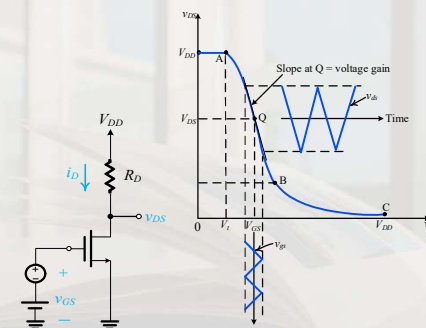


Fig. MOSFET amplifier with a small time-varying signal $v_{gs}(t)$ superimposed on the dc bias voltage V_{GS} .

$$v_{DS} = V_{DD} - i_D R_D$$

$$v_{DS} = V_{DD} - \frac{1}{2} k_n R_D (v_{GS} - V_{tn})^2$$

$$v_{GS}(t) = V_{GS} + v_{gs}(t)$$

$$A_v = \left. \frac{dv_{DS}}{dv_{GS}} \right|_{v_{GS}=V_{GS}} = -k_n R_D (V_{GS} - V_{tn}) = -k_n R_D V_{OV}$$

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Common Source Amplifier

Consider the amplifier circuit shown below. The transistor is specified to have $V_t = 0.4\text{V}$, $k_n' = 0.4\text{ mA/V}^2$, $W/L=10$, $\lambda=0$. Also, let $V_{DD}=1.8\text{V}$, $R_D=17.5\text{k}\Omega$, and $V_{GS}=0.6\text{V}$.

(a) For $v_{gs}=0$ (hence $v_{ds}=0$), find V_{OV} , I_D , V_{DS} , and A_v .

Solution:

$$(a) \quad V_{GS}=0.6\text{V}, V_{OV}=0.6-0.4=0.2\text{V}.$$

$$I_D = \frac{1}{2} k_n' \left(\frac{W}{L}\right) V_{OV}^2$$

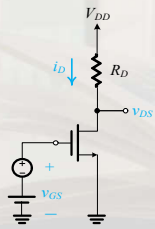
$$= \frac{1}{2} \times 0.4 \times 10 \times 0.2^2 = 0.08\text{ mA}$$

$$V_{DS} = V_{DD} - R_D I_D$$

$$= 1.8 - 17.5 \times 0.08 = 0.4\text{ V}$$

$$A_v = -k_n R_D V_{OV}$$

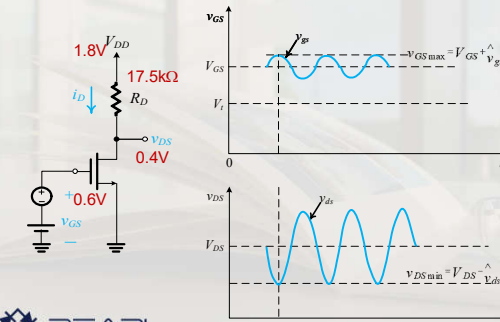
$$= -0.4 \times 10 \times 0.2 \times 17.5 = -14\text{V/V}$$



Continued

(b) Find the maximum allowable amplitude of a sinusoidal v_{gs} .

Solution:



(b) Since $V_{OV} = 0.2\text{V}$ and $V_{DS} = 0.4\text{V}$

$$v_{DSmin} \geq v_{GSmax} - V_t$$

$$0.4 - |A_v| \hat{v}_{gs} \geq 0.6 + \hat{v}_{gs} - 0.4$$

$$\hat{v}_{gs} \leq \frac{0.2}{|A_v|+1} = 13.3\text{mV}$$

Maximum Input Signal Amplitude

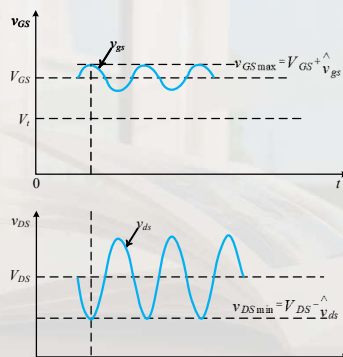


Fig. Signal waveforms at gate and drain for the amplifier

■ To keep the MOSFET in saturation region:

$$v_{DSmin} \geq v_{GSmax} - V_{tn}$$

Graphical Analysis with Load Line

■ **Load line:**

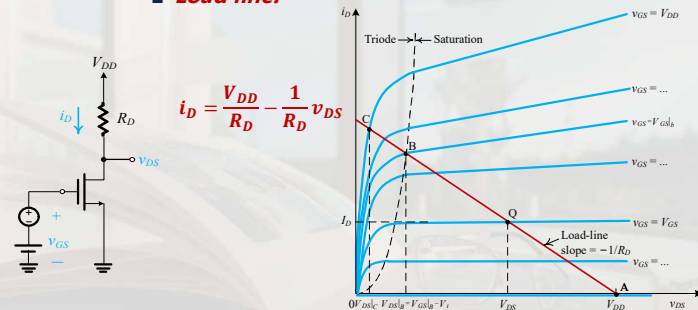
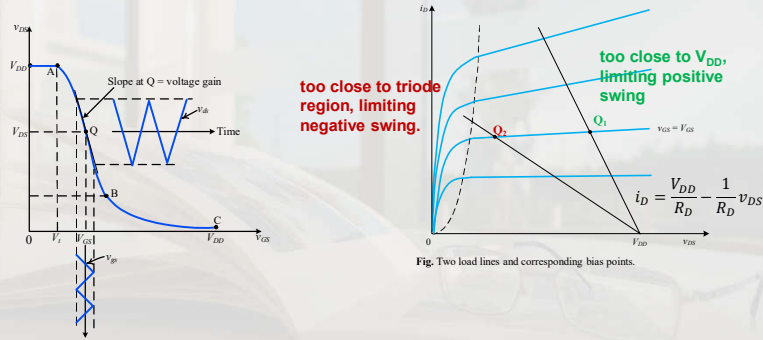


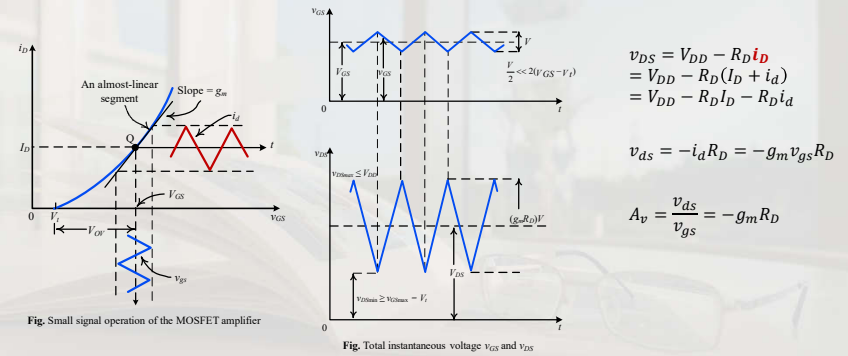
Fig. Graphical construction to determine the voltage-transfer characteristic of the amplifier

Consideration for Bias Point



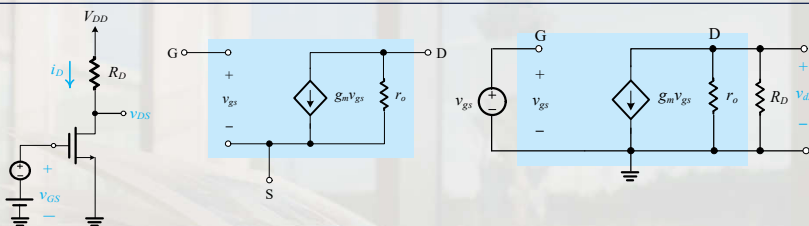
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Voltage Gain



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MOSFET Small Signal Model



- In small signal AC analysis, **DC voltage source = short circuit**

$$A_v = \frac{v_{ds}}{v_{gs}} = -g_m (R_D || r_o)$$

- The equivalent circuit is valid for both NMOS and PMOS

- In **PMOS**, use **absolute sign** for all parameters: $|V_{GS}|$, $|V_{t}|$, $|V_{OV}|$, $|V_A|$, and replace k_n with k_p

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Output Resistance and Transconductance

Output resistance at drain:

$$r_o = \frac{|V_A|}{I_D}$$

Transconductance:

$$i_D = I_D + i_d = \frac{1}{2} k_n (V_{GS} + v_{gs} - V_{tn})^2$$

$$= \frac{1}{2} k_n (V_{GS} - V_{tn})^2 + k_n (V_{GS} - V_{tn}) v_{gs} + \frac{1}{2} k_n v_{gs}^2$$

$$i_d = k_n (V_{GS} - V_{tn}) v_{gs}$$

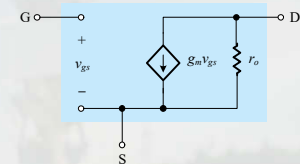
Or

$$g_m \equiv \frac{\partial i_D}{\partial v_{GS}} \bigg|_{v_{GS}=V_{GS}}$$

$$g_m = \frac{i_d}{v_{gs}} = k_n (V_{GS} - V_{tn}) = k_n V_{OV}$$

$$V_{OV} = \sqrt{2I_D / k_n} = \sqrt{2I_D / (k_n' W/L)}$$

$$g_m = \sqrt{2k_n' W/L} \sqrt{I_D}$$



Or

$$g_m = k_n V_{OV} = k_n' (W/L) V_{OV}$$

Or

$$g_m = \frac{2I_D}{V_{GS} - V_{tn}} = \frac{2I_D}{V_{OV}} = \frac{I_D}{V_{OV}/2}$$

Three **design parameters**: W/L , V_{OV} , and I_D .

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