EE270: Homework 2

Problem 1

A certain boost converter is implemented with a MOSFET and a p–n diode. The MOSFET can be modeled as ideal, but the diode exhibits a substantial reverse-recovery process, with reverse recovery time t_r and recovered charge Q_r. In addition, the inductor has winding resistance R_L.

(a) Derive an equivalent circuit that models the dc components of the converter waveforms and that accounts for the loss elements described above.

(b) Solve your model to find an expression for the output voltage.

(c) Plot the output voltage vs. duty cycle over the range $0 \leqslant D < 1$, for the following values: $R_L = 0.4\Omega$, $f_s = 200\text{kHz}$, $Qr = 8\mu\text{C}$, $t_r = 100\text{ns}$, $R = 60\Omega$, $V_g = 24\text{V}$.

Problem 2

An unregulated dc input voltage V_g varies over the range $40\text{V} \leqslant Vg \leqslant 80\text{V}$. A buck converter reduces this voltage to 28V; a feedback loop varies the duty cycle as necessary such that the converter output voltage is always equal to 28V. The load power varies over the range $10\text{W} \leqslant P_{load} \leqslant 1000\text{W}$. The element values are:

$$L = 18\mu\text{H} \quad C = 470\mu\text{F} \quad f_s = 50\text{kHz}$$

Loss may be ignored.

(a) Over what range of V_g and load current does the converter operate in CCM?

(b) Determine the maximum and minimum values of the steady-state transistor duty cycle.

Problem 3

DCM conversion ratio analysis of the SEPIC converter of Fig. 1.

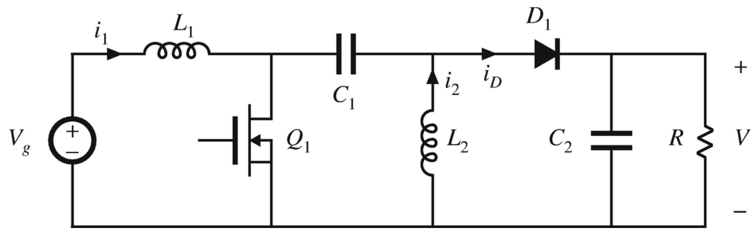

Figure 1: SEPIC converter.

(a) Suppose that the converter operates at the boundary between CCM and DCM, with the following element and parameter values:

$$
\begin{array}{ll}
D = 0.225 & f_s = 100\text{kHz} \\
V_g = 120\text{V} & R = 10\Omega \\
L_1 = 50\mu\text{H} & L_2 = 75\mu\text{H} \\
C_1 = 47\mu\text{F} & C_2 = 200\mu\text{F}
\end{array}
$$

Sketch the diode current waveform $i_D(t)$, and the inductor current waveforms $i_1(t)$ and $i_2(t)$. Label the magnitudes of the ripples and dc components of these waveforms.

(b) Suppose next that the converter operates in the discontinuous conduction mode, with a different choice of parameter and element values. Derive an analytical expression for the dc conversion ratio $M(D, K)$.

(c) Sketch the diode current waveform $i_D(t)$, and the inductor current waveforms $i_1(t)$ and $i_2(t)$, for operation in the discontinuous conduction mode.

Problem 4

Analysis of the DCM flyback converter. The flyback converter of Fig. 2 operates in the discontinuous conduction mode.

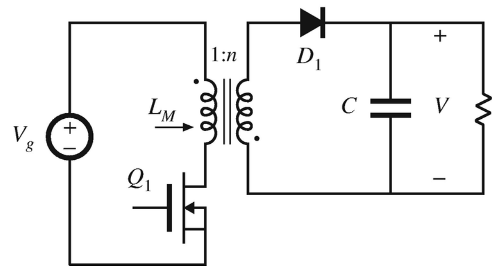

Figure 2: Flyback converter.

(a) Model the flyback transformer as a magnetizing inductance in parallel with an ideal transformer, and sketch the converter circuits during the three subintervals.

(b) Derive the conditions for operation in discontinuous conduction mode.

(c) Solve the converter: derive expressions for the steady-state output voltage V and subinterval 2 (diode conduction interval) duty cycle D_2.

Problem 5

Optimal reset of the forward converter transformer. As illustrated in Fig. 3, it is possible to reset the transformer of the forward converter using a voltage source other than the dc input V_g; several such schemes appear in the literature. By optimally choosing the value of the reset voltage V_r, the peak voltage stresses imposed on transistor Q_1 and diode D_2 can be reduced. The maximum duty cycle can also be increased, leading to a lower transformer turns ratio and lower transistor current. The resulting improvement in converter cost and efficiency can be significant when the dc input voltage varies over a wide range.

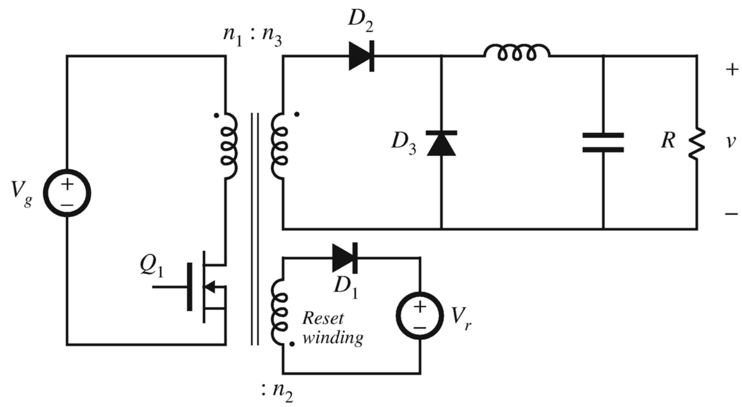

Figure 3: Forward converter with auxiliary reset winding.

(a) As a function of V_g, the transistor duty cycle D, and the transformer turns ratios, what is the minimum value of V_r that causes the transformer magnetizing current to be reset to zero by the end of the switching period?

(b) For your choice of V_r from part (a), what is the peak voltage imposed on transistor Q_1?

This converter is to be used in a universal-input off-line application, with the following specifications. The input voltage V_g can vary between 127 and 380 V. The load voltage is regulated by variation of the duty cycle, and is equal to 20 V. The load power is 480 W.

(c) Choose the turns ratio n_3/n_1 such that the total active switch stress is minimized. For your choice of n_3/n_1, over what range will the duty cycle vary? What is the peak transistor current?

(d) Compare your design of Part (c) with the conventional scheme in which $n_1 = n_2$ and $V_r = V_g$. Compare the worst-case peak transistor voltage and peak transistor current.

(e) Suggest a way to implement the voltage source V_r. Give a schematic of the power stage components of your implementation. Use a few sentences to describe the control circuit functions required by your implementation, if any.

Transients and simulation

Shown in Fig. 4 is a diagram of a circuit used to generate a large pulsed magnetic field. The capacitor is pre-charged to a voltage Vx, which can be between 0 and 1500 V. At time $t = 0$, the switch S is closed to trigger the magnetic pulse. The value of R is $100m\Omega$, C is 180μF, and L is 13μH. The switch S and diode D are ideal.

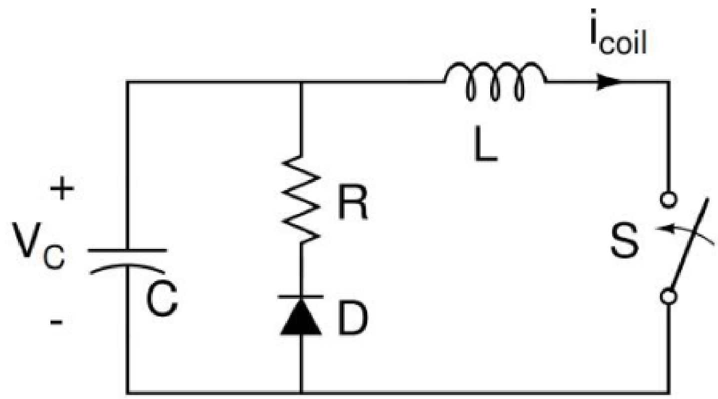

Figure 4: A circuit used to generate a large pulsed magnetic field.

Calculate the following:

(a) The time response of the coil current (i_{coil}) after the switch S is closed, as a function of the pre-charge voltage V_x.

(b) The peak coil current for $V_x = 1500$V.

(c) The time t_1 at which diode D turns on.

(d) The energy dissipated in the resistor R for $V_x = 300$V.

(e) Simulate the circuit operation in Simulink. Plot the corresponding inductor current and capacitor voltages versus time. Attach a print-out of these two state variables to your problem set.

(f) Increase the resistor R until you observe an underdamped response of the system. Turn in a plot of the inductor current and capacitor voltage.

In the Simulink simulation, use "Simscape-SimPowerSystem-Specialized Technology" library to build this circuit.