EE270 Project
Small-Signal Modeling of Four-Switch Buck-Boost Converter with Peak Current Mode Control

1 Introduction

The four-switch Buck-boost (FSBB) converter, as a non-inverting buck–boost converter, has advantages of wide operating voltage range, and capability to step up and down the input voltage. The topology is shown in Fig. 1.

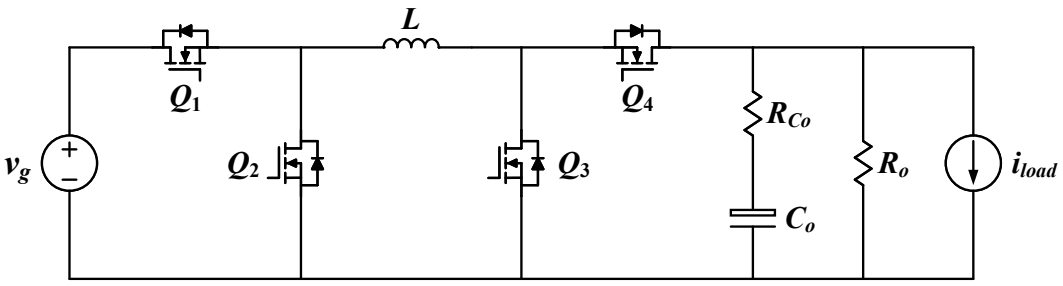

Fig. 1. Basic topology of the FSBB converter.

Current-mode control has been widely used in the power converter design for several decades. Peak current-mode (PCM) control is a kind of current-mode control we have learned in class. As shown in Fig. 2 and 3, PCM control uses a dual-loop structure: an outer voltage loop sets a current reference, while an inner current loop directly limits inductor current peaks. Each switching cycle terminates when the inductor current reaches the reference, enabling cycle-by-cycle current limiting, fast dynamic response, and inherent overcurrent protection. This method simplifies compensation and improves stability compared to voltage-mode control.

Fig. 2 shows a FSBB converter which is ultilized with the PCM control method. The targets of this project are small-signal modeling, loop compensation design, and simulation verification of this closed-loop feedback system.

The circuit parameters of the FSBB converter are listed as follows: $40\,\mathrm{V} \le V_g \le 60\,\mathrm{V}$, $V_o = 48\,\mathrm{V}$, $L = 1\,\mu\mathrm{H}$, $C_o = 500\,\mu\mathrm{F}$, $R_{C_o} = 0.1\,\mathrm{m\Omega}$, $R_o = 1\,\mathrm{k\Omega}$, $R_i = 10\,\mathrm{m\Omega}$, $f_s = 1\,\mathrm{MHz}$. To simplify the work, the other non-ideal parameters not mentioned should not be considered.

The phase shift of its two bridges is also not considered. The operating mode is defined as follows: each switching period contains two subintervals numbered 1 and 2; in the schematic illustrated in Fig. 1, switches Q_1 and Q_3 conduct during subinterval 1 for time DT_s, and switches Q_2 and Q_4 conduct during subinterval 2 for time $(1-D)T_s$.

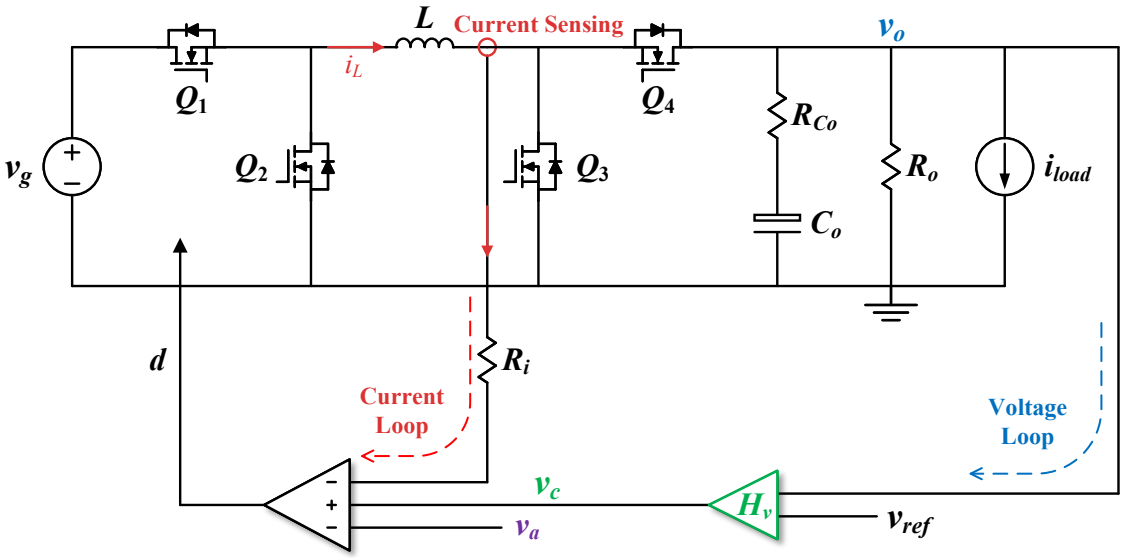

Fig. 2. The closed-loop system of the FSBB converter with PCM control.

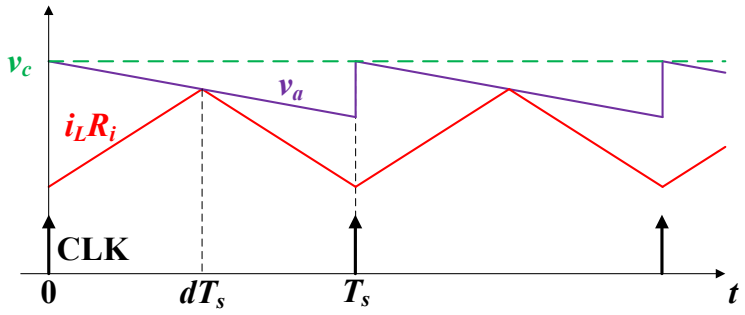

Fig. 3. The modulation scheme of PCM control.

2 Tasks

This project should be completed by finish the following tasks:

Task 1

For the FSBB converter with PCM control, refer to the method shown in Fig. 18.24-18.28 of the class book "Fundamental of Power Electronics", construct a small signal model of the system. Then derive the transfer functions of G_{vc} and G_{vg-cpm}.

Task 2

Set a appropriate slope of the ramp voltage v_a. Design the compensator H_v based on your model. Utilize your design, construct the closed-loop feedback simulation model with given circuit parameters using SIMPLIS. The PCM control structure can be refer to Fig.

18.19 in the class book. The choice of H_v transfer function is not limited. The compensator can be realized by the Op-Amp circuit. Your design needs to be able to run the simulated circuit in steady state with 48 V input.

Task 3

Based on the simulation circuit you built, simulate the control-to-output transfer function G_{vc}. To verify the accuracy of the modeling, compare the simulated result with your modeling result by plotting them into the same figure with different lines and colors as Fig. 4. You need to use Matlab for plotting.

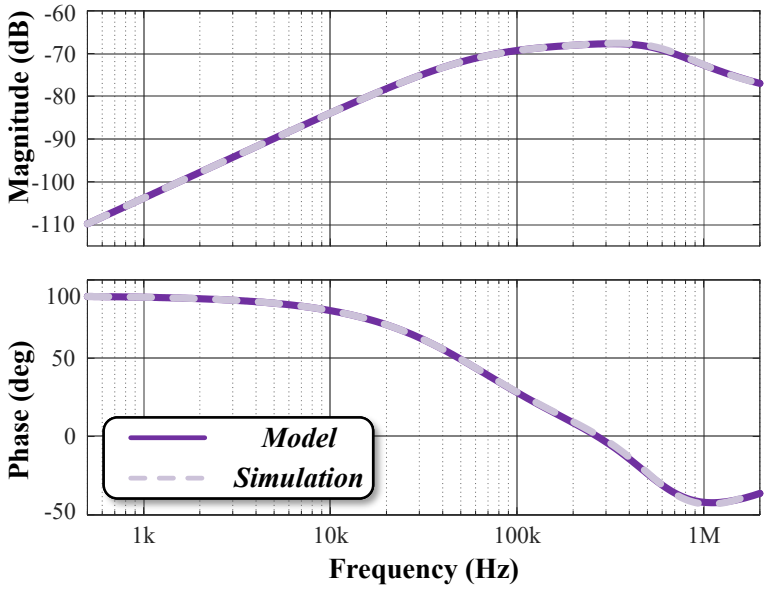

Fig. 4. Example: the simulation verification of the modeling.

Task 4

Optimize your compensation design to enable the system to withstand a load step transient response of 0-20A and a input step transient response of 40-60V. Display your simulated waveforms. As shown in Fig. 5 and 6. For example, your results need to include: Duty ratio d, inductor current i_L, transient parameters i_{load} or v_g, and output voltage v_o.

Discussion

Summarize your work. Analyze the accuracy of your modeling process and compare it with simulation results, and discuss the reasons for the errors in the modeling method you used at high frequencies.

Compare the voltage mode and current mode control. Explain the advantages of current mode control by combining their control-to-output transfer function G_{vc}.

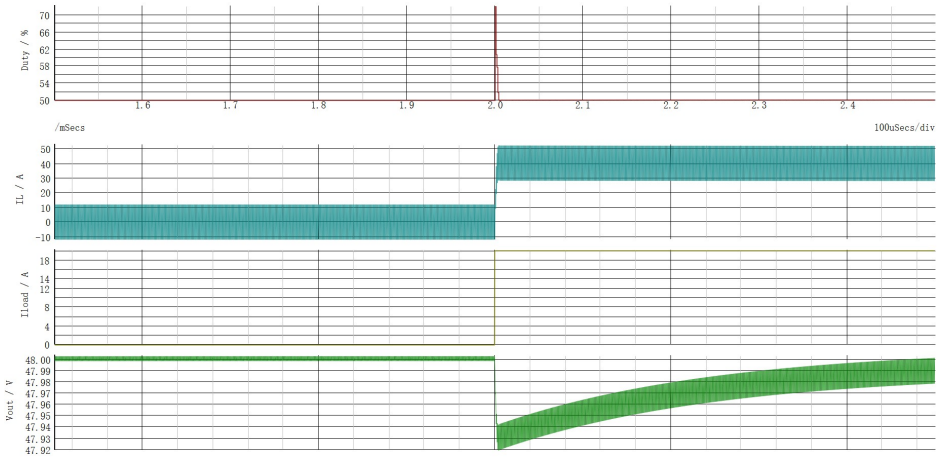

Fig. 5. Example: the simulation of load transient response.

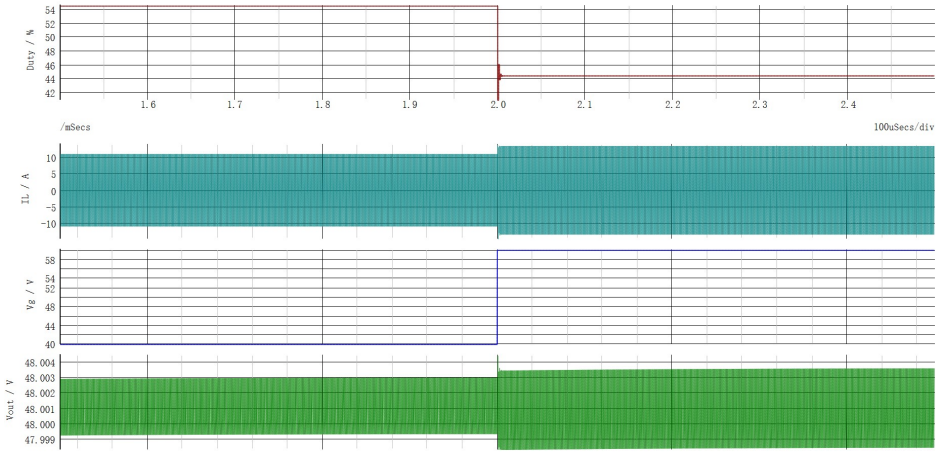

Fig. 6. Example: the simulation of input transient response.

3 Report Requirements

The final report shall contain the following:the following:

1. Complete derivation of system modeling equations
2. Compensator design procedure
3. SIMPLIS schematic diagrams and steady-state operating waveforms
4. Frequency response comparison (modeling vs. simulated)
5. Transient response waveforms with performance metrics
6. Critical analysis of modeling accuracy and high-frequency discrepancies

Submission Guidelines

- Individual submission required – academic misconduct will result in severe penalties
- Submission package must include:
  - PDF report in English (handwriting prohibited)
  - SIMPLIS project files
  - MATLAB scripts
- File naming convention: FirstName-StudentID.zip (e.g., Zhaocheng-2024241025.zip)
- Submit the file to http://10.19.124.26:8000/u/d/920dc96567904bb89cc3/ before DDL
- Late submissions will not be accepted